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Comprehensive Review of Different Methods for Via Filling Process in Through Silicon via (TSV) Fabrication

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Abstract – *Through silicon vias (TSVs) is a promising technology that has been introduced into high volume manufacturing recently. Through silicon via (TSV) can be customized to fit different design specifications, from dimensions to materials to the location of the vias. This paper gives a comprehensive summary of the TSV fabrication steps, including etch, insulation, and metallization process. In addition, recent researches for various methods applied for via filling process also been discussed. Moreover, the current and future prospects of electroless copper deposition as low cost metallization technology for via filling process had been addressed. In conclusion, electroless copper deposition is a promising technique has a bright future development to be implemented for TSV application.* ***Copyright © 2016 Penerbit Akademia Baru - All rights reserved.***

Keywords: Through Silicon Via (TSV), Via Filling, Electroless Cu Plating

I.0 INTRODUCTION

Recently, modern electronic devices are in a constant demand of higher density integration, smaller size, superior performance, and lower cost [1-4]. Traditional 2D integration approaches have been shown to have serious limitations when it comes to fulfilling these demands. Three-dimensional integrated circuit (3D-IC) with through silicon vias (TSVs) is a promising technology to improve performance without increase of power consumption [5,6].

Detail reviews on the technology and manufacturing of TSV have been described by several authors [7,8]. The idea of using TSV technology has been around for many years as it was introduced by William Shockley [9] in 1954. However, only recently the technology has been introduced into high volume manufacturing. A TSV can be customized to fit different design specifications, from dimensions to materials to the location of the vias. They drastically reduce the interconnect length among chips, increasing speed and improving the circuit performance [10]. In the near future, the TSV diameter is expected to be smaller than 2 µm, and the aspect ratio is expected to be larger than 10 [11].

Key technologies involved in the TSV process include (a) silicon (Si) via formation with controlled profile, (b) insulation layer, barrier layer and seed layer deposition with good conformality, and (c) defect-free via filling. Deep reactive ion etching (DRIE) based on the Bosch method is usually used to fabricate the Si vias. This is a time-multiplexed alternating process that alternates etch and passivation steps, each lasting only a few seconds [12]. In 2009,

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Xiaopeng Li et. al. [13] had developed a two-step etching process to fabricate the Si pillar arrays, which are macroporous Si formed by photoelectrochemical etching, and post-chemical KOH etching. The method had been improved by Yuncan Ma and friends [14] in 2013, where he had proposed a simple method using 800-nm femtosecond laser irradiation and chemical selective etching for fabrication of high aspect ratio of all Si groves.

In order to investigated the effect of chemical and mechanical factors on the chemical mechanical polishing (CMP) performance in TSV fabrication, Can Rao et. al. [15] had demonstrated the mechanism on non-uniformity and via dishing. He concluded that high down force and low down force should be combined to achieve a high removal rate as well as low dishing. Wonseop and friends [16] also shared the same objective, but more specifically to understand the effect of pH and down pressure in elucidating the chemical and mechanical mechanism in CMP process. He concluded that the repulsive interaction force, solubility of amorphous silica, and total contact area at the pad-particles-wafer interface are important factors in determining polishing performance.

Some literature has investigated the TSV via filling process with various methods. However, there are some discrepancies in the reported findings, especially on the advantages and disadvantages of various methods for via filling. Therefore, this paper will present an overview of the TSV integration in terms of the fabrication process. Various methods for the metallization of copper (Cu) film deposited on TSV or via filling will be discussed based on researches that had been conducted recently and the advantages and disadvantages of the process was also identified. Moreover, the current and future prospects of electroless copper plating as low cost metallization technology for via filling process will be addressed. In addition, to the author's knowledge, there is still no comprehensive literature on the subject.

2.0 TSV INTEGRATION

The fabrication process of the TSV structure varies depending on the design and application [17]. For instance, partially-filled (annular) and fully-filled TSVs have a different fabrication processes. Also, the structures, such as redistribution lines (RDL) and contact pads, which enable electrical measurement, add the fabrication steps. Currently, there are two different approaches to TSV vertical integration that have been adopted for 3D chip stacking depending on its application type, which are blind via filling before wafer thinning (via-first approach) and through via filling after wafer thinning (via-last approach) [18,19].

In via first approach, vias are filled with Cu from the front side of the Si wafers by electrodeposition process. After vias are filled, overburden is removed and the wafer is thinned at the backside of the wafer until the TSV interconnects are exposed. Meanwhile in via last approach, vias are filled after wafer thinning. Seed layer is deposited on one side of the wafer and a carrier wafer may be used to handle this thin wafer. The bottom electrode could be sputtered metals on polymers and remove the polymer to form the film type bottom electrode or just direct metal to metal bonding. Fig. 1 shows the schematic diagram for via first and via last approaches.

Journal of Advanced Review on Scientific Research
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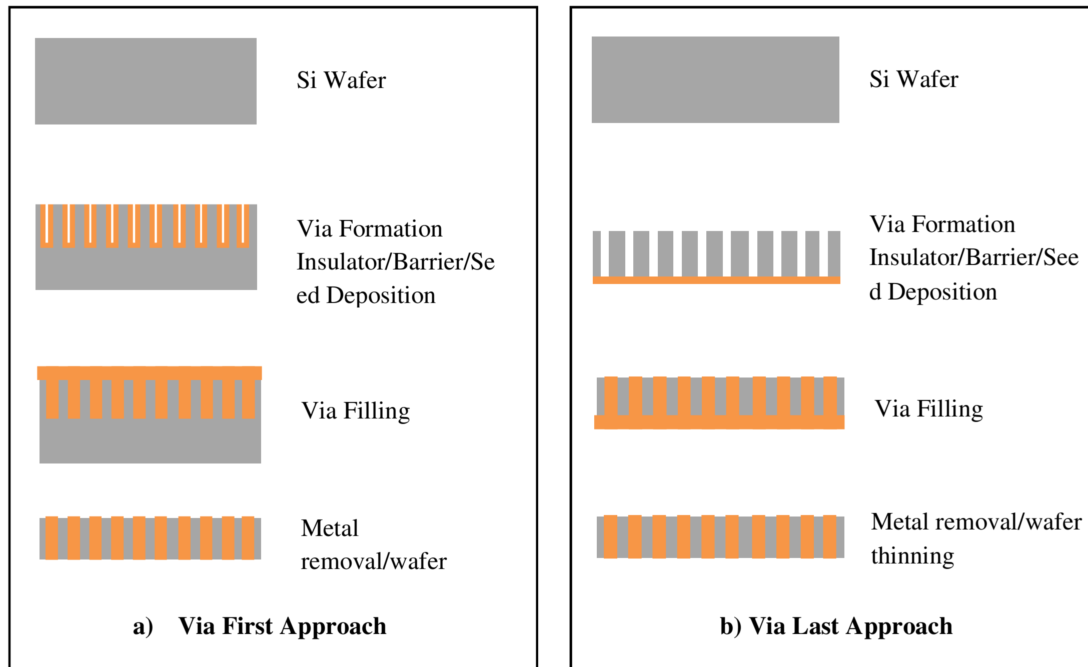

Figure 1: (a) Via First and (b) Via Last Approaches Process [19]

Due to the difficulties in handling and plating thin wafers, the first approach gained much popularity becoming the most preferred TSV stacking method in industry today [19]. The key technologies enabling TSV-based 3D chip integration, based on the via first approach process is summarized as follows. Study on via first approach process optimisation had been conducted by Cyrille Laviron [20] and details of process are can be referred in reference [21].

2.1 Via formation

DRIE is generally used to create via holes [22]. This process is a series of etch and deposition cycles, each lasting only a few seconds, which uses sulphurhexafluoride (SF_6) to rapidly etch the Si and fluorocarbon to passivate the sidewalls of the via during a time-multiplexed deep etching process. The Bosch process etches with high selectivity, achieves near-vertical sidewalls, and leaves small sidewall scallops [22].

2.2 Insulator/barrier/seed deposition

Si via sidewall need to be passivated to electrically isolates the TSV from the surrounding Si substrate. Good insulation properties with higher breakdown voltage, no leakage, and no cracking are important for via lining dielectric materials [23]. Other important criteria for via lining dielectrics are good coverage and uniformity, lower stress and process temperature compatibility [23].

Silicon dioxide (SiO_2) layer is commonly used as via lining dielectric material, which is highly conformal. Organic polymer can be used as via lining dielectric materials as well. Among the organic via liner materials, parylene is highly conformal, which is deposited in a special parylene deposition chamber. [23]

Journal of Advanced Review on Scientific Research
ISSN (online): 2289-7887 I Vol. 17, No.1. Pages 8-12, 2016

The process followed by the fabrication of diffusion/barrier layer which can be made from silicon nitride (Si_3N_4), titanium nitride (TiN) or tantalum nitride (TaN). The thickness of the insulation layer is about 1-2 μm whereas the thickness of the diffusion layer is in the range of 5-20 nm. Both of these layers can be deposited with the plasma-enhanced chemical vapor deposition (PECVD). SiO_2 layer can be also deposited with wet thermal oxidation process. For barrier or seed layer deposition, atomic layer deposition (ALD), physical vapor deposition (PVD) or CVD can also be used, depending upon feature shape and aspect ratio. ALD produces highly conformal layers and it allows the deposition in the low temperatures. The PVD process has the advantages of low process temperature and fair adhesion, but poor uniformity, whereas the CVD process has moderate process temperature and good uniformity, but poor adhesion. [24]

2.3 Via filling process

There are typically three types of via deposition process, such as lining, full lining, as well as full lining with stud formation [24], as illustrated in Fig. 2.

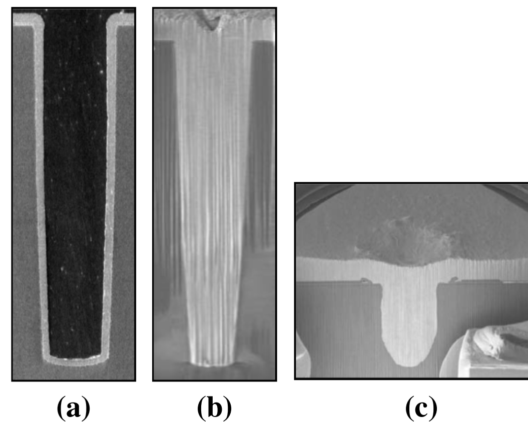

Figure 2: Types of via deposition process; a) lining, b) full lining, and c) full lining with stud formation. [24]

The lining process is generally used for some sensor applications. Typically, requirement for Cu lining are high degree of conformality and thickness of 5-15% of the feature width. Meanwhile, full lining is employed over a wide range of feature dimensions, from near damascene-scale features to large features used for sensor applications. The general requirement for full lining is a robust and void-free deposition within the features. The choice of adding a photo defined resist mask allow the creation of a Cu stud on top of the filled via depends on the integration scheme and the tradeoff between CMP removal of Cu overburden and chemical etch of the barrier and seed layer [24].

To adequately fill vias, a superconformal fill mechanism, where the rate of deposition is faster at the bottom of feature than at the top, is required.

2.4 Electrodeposition of RDL

RDL can be plated for rerouting the current paths. Compared to typical bump patterns, RDL patterns are generally much more complicated, the deposit thickness is much thinner (typically <7 μm), and the specification for thickness uniformity is more stringent.

Journal of Advanced Review on Scientific Research
ISSN (online): 2289-7887 | Vol. 17, No.1. Pages 8-12, 2016

2.5 Wafer thinning and bonding

Final wafer thickness is usually below 70 µm, thinned by a combination of grinding/lapping, CMP wet etching and dry etch. The challenges for grinding-based thinning process are the difficulty in handling thinned wafers and the creation of micro-cracks and chipping due to the formation of a sharp edge profile. A variety of bonding methods are available, including Si fusion bonding, polymer adhesive bonding, metal-to-metal bonding and eutectic bonding.

3.0 VARIOUS METHODS APPLIED FOR VIA FILLING PROCESS

The TSV filling technique is an important factor in the TSV interconnection process. There are different methods for the metallization process such as CVD, PVD, electrodeposition and electroless deposition process.

Yann Civale et al. (2013) [25] investigated the thermal stability of PVD diffusion barrier in 3D TSV process. Through his study, he concluded 5 nm PVD Ta barriers are thermally stable, while PVD Ti-barriers require thicknesses above 5 nm to guarantee their thermal stability. Unfortunately, as the TSV density and aspect ratio increase, PVD technique is not sufficient to overcome issues coming from deposition step coverage and continuity.

In 2014, Larissa Djomeni et al [26] conducted investigation on a barrier layer for Cu diffusion in high aspect ratio TSVs using a different method which was a low temperature MOCVD deposition. Earlier to that, a novel study had been conducted by John A.T. Norman [27] in 2008 to investigate new precursors (KI3 and KI5) for CVD Cu metallization in TSV fabrication process. These new precursors are thermally stable yet chemically reactive under CVD conditions, growing Cu films of exceptionally high purity at high growth rates. Their thermal stability can allow for elevated evaporation temperatures to generate the high precursor vapor pressures needed for deep penetration into high aspect ratio TSV vias. In the same year, Druais et al. [28] demonstrated the fabrication of 10:1 vias with a diameter of 5 m through a batch CVD deposition of a TiN barrier and then an electrografting deposition of a Cu seed layer. M. J. Wolf [29] also investigated the impact of seed layer nature on filling ratio and void formation with respect to via diameter and via depth. He used different approach and different types of materials for the seed layer process which are CVD Cu seed layer, CVD tungsten seed layer, sputtered TiW/Cu seed layer and CVD Tungsten and sputtered TiW/Cu seed layer. However, the CVD process temperature was higher than 500 ◦C and the resistivity of the TiN layer was controlled by means of a toxic NH_3 gas flush step, which restrained this method from the practical application.

The specificity of TSV structures, combining both high aspect-ratios and via depth ranging from tenth to several hundred microns, implies the development of new deposition methodologies and chemistries. In recent years, the development of Cu plating technology for TSV via filling has been a focus within the 3D integration community.

In 2006, Bioh Kim [30] investigation was focused on developing methodologies to avoid voids and seam during Cu filling of deep vias through electrodeposition process. He found that the plating bath for via filling requires a high metal concentration and a strong-super conformal capability. He also concluded that reducing current crowding at the via bottom by optimizing deposition conditions is critical in achieving void-free, bottom-up filling.

Journal of Advanced Review on Scientific Research
ISSN (online): 2289-7887 I Vol. 17, No.1. Pages 8-12, 2016

His agreement was supported by Dean Malta [31] and K. Y. K. Tsui [32] who both studied on electrodeposition for TSV via filling process in year 2009. Dean Malta [31] added a specific key plating factors that need for a careful attention in electrodeposition process, which are the optimization of the seed layer and the prewet process, the solution additive levels and plating current density. Meanwhile, K.Y.K. Tsui [32] mentioned that the key factors that influencing the via filling quality are the variation in both via opening and depth, current density, power waveform and so on. Study on the seed layer process also had been conducted by Sanghoon Jin [33] currently using alkaline pyrophosphate solution in electroplating process.

For electrodeposition process in particular, the mode of action of organic additives (accelerator, suppressor and leveller) promoting the so-called ‘‘bottom-up filling” can be greatly affected by mass transportation and convection effects associated with large volumes TSV vias. The relative concentrations between these three additives play an important role for the via filling, promoting the bottom-up effect, also called superfilling. The understanding of the action of each additive, particularly for the superfilling generation, was widely studied.

In 2010, Elise Delbos [34] had optimized the bottom up filling for efficient Cu metallization in TSV. **Fig. 3** shows the via filling cross-sections as a function of accelerator concentration. Concerning the via surface, the Cu layer thickness remains constant at about 8 μm despite the accelerator quantity increase. Therefore, she concluded that the high efficiency of the levelling and suppressing agents allowing the superfilling in the structure to be modified without leading to undesirable thick deposits on the wafer surface. Her study was agreed by Haiyong Cao [35] who studied the Cu filling mechanism by the simulation of electric field distribution in 2014.

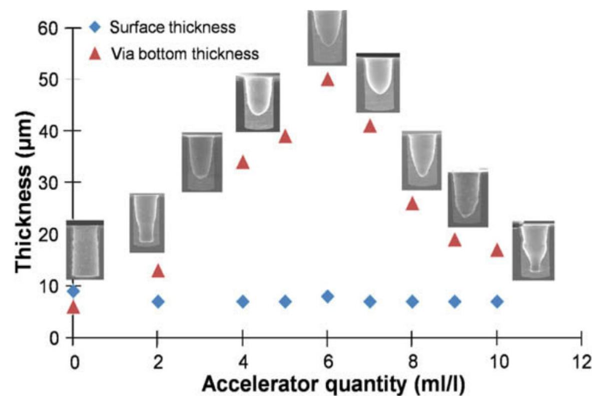

Figure 3: Via filling cross-sections as a function of accelerator concentration [34]

Although the superconformal growth is well-established in electrolyte with optimal additives concentration, the use of plating additives will induce high process complexity in terms of process control and high process costs due to the high consumption of the additives. In addition, void-free Cu deposition in TSVs is still a challenge. When the Cu was deposited in the vias, the electrolyte cannot wet the vias surface completely and in deep and narrow vias even does not reach some local vias points. Due to the insufficient wetting of TSVs, electroplating remains open at incomplete wetting local points, which leads to the void formation and poor electrical performance.

In order to overcome the problem of void formation and to achieve uniform and void free deposition in TSVs, Few studies on improving the wetting surface of Cu seed layer in TSVs had been conducted.

Journal of Advanced Review on Scientific Research
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Predeep Dixit et al. [36] reported various surface treatment methods such as plasma, UV and wet treatment to improve the wetting characteristics of vias sidewall surface and through-wafer Cu interconnects of aspect ratio as high as 20. This is in agreement with Junhong Zhang [37] who had focussed on the investigation of wetting process of Cu filling by agitation and vacuum pretreatment in 2015. By agitation pretreatment, a large void was observed at the bottom of the vias where the Cu seed layer was clearly seen, which was attributed to the insufficient wetting of vias. The vacuum pretreatment results suggested that the air inside the vias was almost completely evacuated, which was also agreed by Li Du et. al. [38], as shown in Fig. 4. Hence, the deionized water used as wetting solution easily permeated the blind vias relying on atmospheric pressure. Consequently, the uniform, complete and void-free Cu filling was achieved due to better wettability of 273K deionized water.

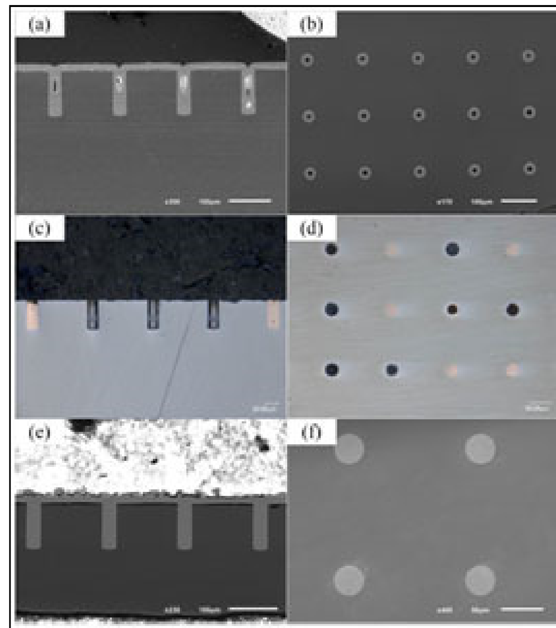

Figure 4: The influence of the pre-wetting methods on Cu filling. (a and b) The cross-section and surface views of the Cu filled vias after rocking agitation. (c and d) The cross-section and surface views of the Cu filled vias after ultrasonic agitation. (e and f) The cross-section and surface views of the Cu filled vias after vacuuming. [38]

4.0 ELECTROLESS CU DEPOSITION AS AN ALTERNATIVE METHOD

Although electrodeposition is now commonly used as the filling technique, it is not the only one. Another promising candidate for TSV filling is electroless plating (ELP), which was first observed by Wurtz [39] in 1844. It is a non-galvanic type of plating that involves several simultaneous reactions in an aqueous solution, which occur without the use of external electric power. The reaction is accomplished when hydrogen is released by a reducing agent, and oxidized thus producing a negative charge on the surface. For this reason, no electrode is needed for the plating. Moreover, because of its low temperature, wafer size flexibility, low equipment costs and conformal deposition property, it finds applications in IC fabrication.

Journal of Advanced Review on Scientific Research
ISSN (online): 2289-7887 | Vol. 17, No.1. Pages 8-12, 2016

Few studies had been conducted recently on the TSV via filling process by means of electroless plating technique. In 2003, Hidemi Nawafumi [40] had investigated the improvement of via-filling in neutral electroless Cu plating for ULSI metallization. From his investigation, he found out that a minute contact hole can be filled with Cu without causing a seam. This finding was supported by Jaehui Ann [41] in her investigation of Cu electroless plating on the sidewall of the through-wafer via holes. Meanwhile in 2012, F. Inoue [42] had formed a conformal diffusion barrier and seed layers by electroless plating using palladium nanoparticles (Pd-NPs) catalyst in high aspect ratio TSVs. Later in 2013, he continued the study with feasibility of a TSV filling process using electroless deposition of Cu on atomic layer deposition of ruthenium [43].However, these works were more focus on the pre-deposition treatment of the surfaces which is the deposition of barrier layer or seed layer.

Meanwhile, Santagata et al. [44] presented TSV filling by Cu electroless plating (ELP), as shown in Fig. 5. This method produces uniform fillings and in a shorter time than electrodeposition process. This is because the electroless deposition process happens selectively on desired locations. This feature becomes even more important when the diameter of via decreases. Furthermore, the method enables low cost and low temperature fabrication process.

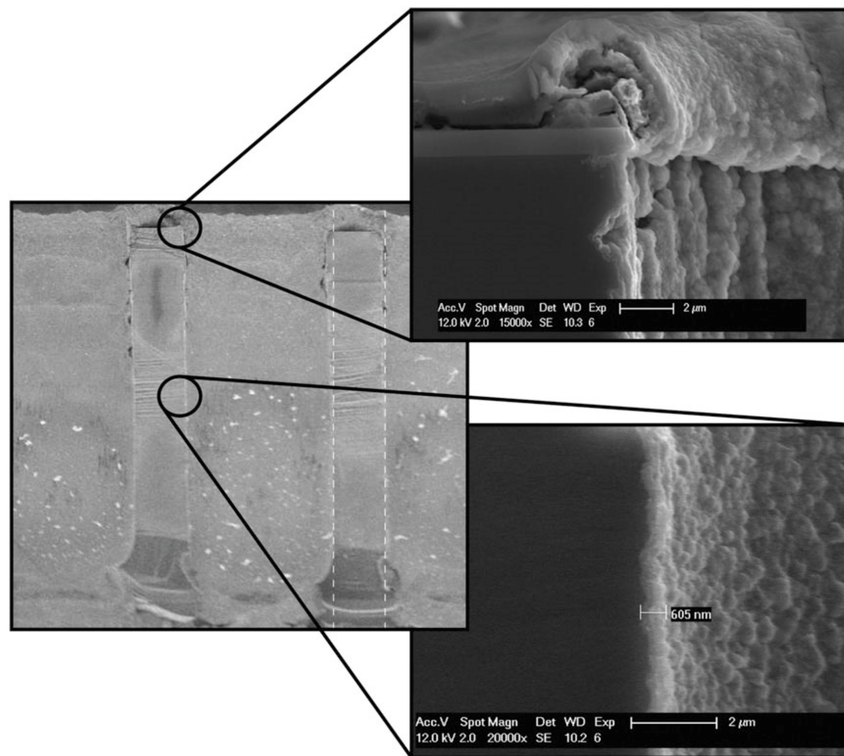

Figure 5: SEM cross section pictures of the TSVs after the electroless deposition of Cu [44]

5.0 CONCLUSION

Journal of Advanced Review on Scientific Research
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The idea of using TSV technology has been around for many years. However, this technology has only recently been introduced into high volume manufacturing. This paper presented an inclusive review of various methods for via filling process in TSV fabrication. The key technologies enabling TSV-based 3D chip integration was summarized. Furthermore, electroless Cu deposition had been identified as current alternative method for via filling process. It is expected that this will be an active area for research and development for many years.

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