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Harmonic Reduction in Asymmetric Multilevel Inverters: A Dual Modulation Approach

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ABSTRACT

This paper addresses the challenge of optimizing the performance of asymmetric reduced multilevel inverters (ARSMLI) by achieving a compact inverter size while maintaining its output quality. The study examines the effectiveness of two modulation strategies: Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) in low frequency operation and Multicarrier Pulse Width Modulation (MCPWM) in high frequency operation. The ARSMLI is modelled and simulated for 15 and 19-level inverters using the same circuit configuration, but with different DC source ratings. Simulation studies were conducted in PSIM software to evaluate the inverter performance using SHEPWM achieved through PSO-based optimization with a variable modulation index. The assessment is then repeated for MCPWM methods, such as Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD). The main performance parameters: total harmonic distortion (THD) and output voltage quality, are analysed. The results show that APOD of MCPWM produced the highest output quality with the lowest THD, making it the optimal option for ARSMLI applications. In contrast, while SHEPWM provides efficient switching for a low frequency modulation, it cannot produce comparable THD. Nonetheless, both modulation strategies maintain THD performance below 5% in compliance with the IEEE 519 standard.

1. Introduction

Recent advances in multilevel inverters (MLIs) for renewable energy, especially in handling multiple sources of renewable energy (RES) such as photovoltaic (PV) systems and wind turbines, have enhanced their significance in power electronics [1]–[4]. This is attributable to their ability to produce high-quality voltage with low-rating circuits [5]–[8], making MLIs suitable for grid-connected applications. As the demand for efficient and reliable power conversion increases, there is a constant drive to improve MLI topologies and modulation strategies. One such development is the asymmetric reduced-switch multilevel inverter (ARSMLI), which reduces the number of switches and cost while maintaining MLI performance [9], [10].

In MLI, modulation techniques broadly categorised into two types: fundamental switching frequency and high switching frequency [11], [12]. Techniques like Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) involve togging switches On and Off multiple times per cycle in low frequency applications. Its major advantage is that this modulation technique can minimise total harmonic distortion (THD) by removing certain lower-order harmonics, reducing the requirement for

substantial filter hardware in an MLI circuit [13]–[15]. This method solves nonlinear equations to determine the optimal switching occurrence, achieving a significant reduction in THD when operating at low switching loss. Arulappan *et al.* and Behbahanifard *et al.* implementing SHEPWM in their proposed inverter and the studies conclude that the SHEPWM method improved the inverter efficiency [16], [17]. This method is appropriate for solving nonlinear equations as long as the computational resources are available. The method has a disadvantage in its complex calculation and the necessity to recalculate the switching angle if the operating conditions vary.

In contrast, high switching frequency techniques such as MCPWM, use multiple carrier signals to generate a PWM signal for the inverter switch. MCPWM includes several variations, such as Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD) [18]. This high frequency operation helps in achieving a smooth output waveform with lower harmonic content as performed by Iderus *et al.*, Guo *et al.* and Yadav *et.al* in [19]–[21]. But this method come at the cost of increased switching loss and higher electromagnetic interference (EMI). Besides, the switching rate frequency puts greater stress on the switching device, which can affect the lifespan and reliability of the device. Despite these drawbacks, MCPWM's ability to deliver high-quality voltage waveforms with low THD makes it an attractive choice for applications where output voltage quality is of greater importance than inverter efficiency.

Therefore, this paper aims to provide dual-simulation analysis of low-frequency and high-frequency modulation techniques for the ARSMLI. The two different modulation techniques are the SHEPWM, a low frequency modulation and a high frequency modulation, MCPWM. By examining performance such as THD, switching loss, efficiency and output voltage quality under both SHEPWM and MCPWM, this study highlights the strengths and limitations of each approach. These findings are expected to offer insights into selecting suitable modulation strategies for specific power electronics applications, balancing the trade-offs between harmonic performance, efficiency, and circuit complexity.

2. Modulation Strategy

The selected modulation techniques can significantly affect the MLIs' performance especially its inverter output quality. A comparative study of different modulation techniques reveals differences in their effectiveness in minimizing THD.

2.1 Selected Harmonic Elimination Pulse Width Modulation (SHEPWM)

SHEPWM is one of the modulation techniques used in this study to improve MLI's output quality. This low frequency modulation technique requires solving a complex nonlinear equation derived from the mathematical representation of the inverter output voltage, in order to project the switching angle for each multilevel voltage step. It can be accomplished by targeting certain low order harmonics to be eliminated with a finite number of iterative variables such as the modulation index. It could be notice that the modulation indices play the important role in order to project the output voltage close to the optimal value in relation to the inverter's output fundamental voltage component, V_1. The SHEPWM implementation presented in this study using three modulation indices, M_i of 0.6, 0.8 and 1.0. Figure 1 depicts a synoptic diagram of the SHEPWM technique used in the MLI system.

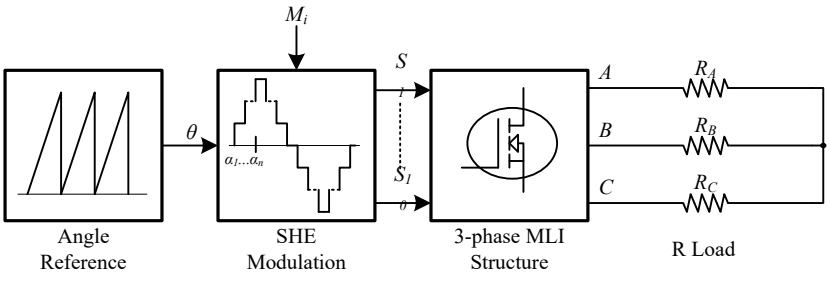

Fig. 1. Synoptic diagram of fundamental frequency modulation technique, SHEPWM.

For a three-phase MLI application, the output voltage equation, V(t) can be represented as in Eq. [1] to Eq. [2],

$$V_{AN} = \sum_{n=1,5,7,11,13,17\ldots}^{\infty} \frac{4V_{DC}}{n\pi}(V_{DCi}cos(n\alpha_i)) \quad (1)$$

$$V_{AN}(t) = V_1(t) + V_5(t) + \cdots + V_n(t) \quad (2)$$

where;

V_{DC} is voltage of DC source,

V_1 is a fundamental voltage of the *F*(t) spectrum,

and *i* is switching angle sequence by integer constraint $0 \leq i \leq n$

To eliminate certain harmonics while retaining the fundamental component of the output voltage in a three-phase MLI, the triplen harmonic is first assumed cancelled out in the line-to-line voltage. As a result, the most significant lower-order harmonics causing higher THD will be eliminated. For example, in a 15-level MLI, the SHEPWM could mitigate up to 6 targeted undesired harmonics, and in a 19-level MLI, this method could eliminate up to 7 targeted undesirable harmonics. In this paper, a numerical metaheuristic approach based on Particle Swarm Optimization (PSO) is used to solve the output voltage equation by setting the objective function and the Fourier coefficients of the undesirable harmonic to zero.

2.2 Multicarrier Pulse Width Modulation (MCPWM)

MCPWM is a high-frequency modulation technique that generating PWM signals by comparing multiple carrier signals to the reference signal. There are three common methods in MCPWM: Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition. The characteristics of the multicarrier signals distinguished by these methods. As illustrated in Figure 2, in PD, all carrier signals are in phase, whereas in POD, carrier signals above and below the reference are 180 degrees out of phase, and in APOD, the carrier signals alternate between in-phase and 180 degrees out of phase.

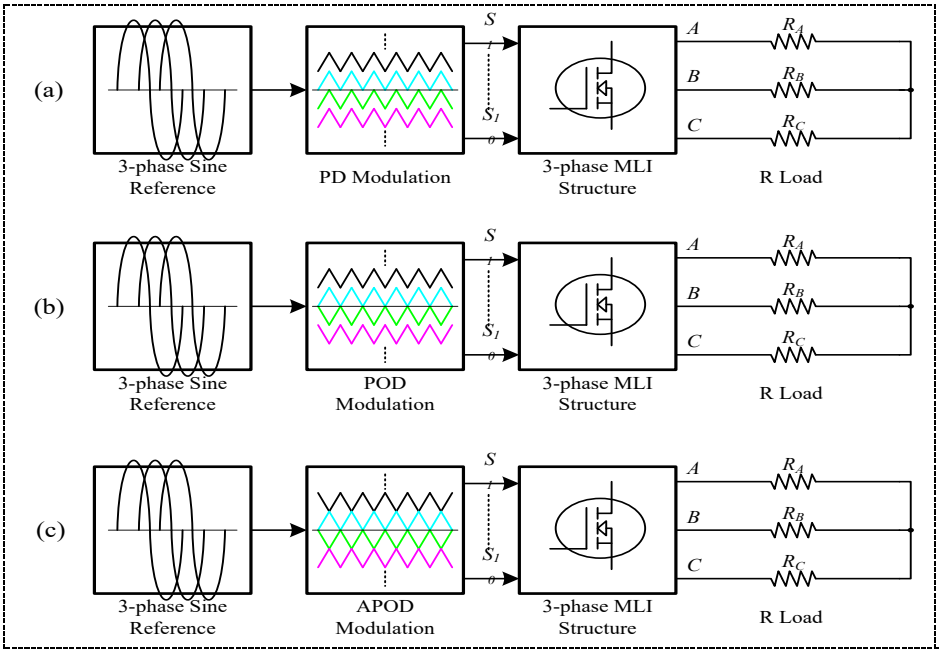

Fig. 2. Synoptic diagram of high frequency modulation technique, level shifted multi-carrier PWM; (a) PD, (b) POD, and (c) APOD

This paper showcases three common types of the MCPWM method. All these methods generate different PWM signals by comparing high frequency multiple carrier signals to a reference signal in fundamental frequency. The stacked count of the multi-carrier signal refers to the desired multilevel output step. Each method uses a different phase configuration for their multi-carrier signal, hence, the intersection points determine the switching instances for each modulation set.

3. Configuration of the Proposed Asymmetrical RSMLI

Figure 3(a) depicted the basic module of the proposed ARSMLI topology. The proposed configuration gives flexible switching and more adaptable to produce a different level of MLI output. As illustrated in Figure 3(b), the modular multiplication of submodules enables potential circuit scalability.

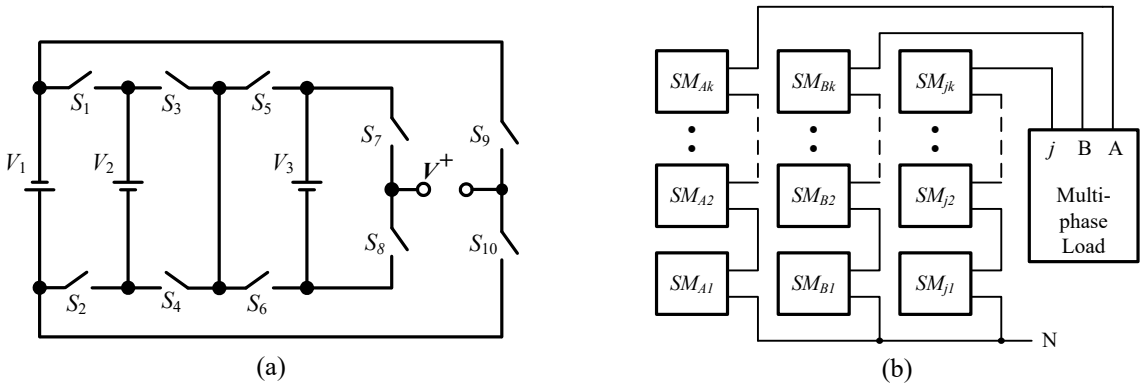

Fig. 3. (a) Schematic of the scalable ARSMLI, (b) Possible higher level MLI generation by *k* sub-module multiplication and *j* phase application setup

Since MLIs can be reconfigured to accommodate various DC source combinations, a reduced-switch MLI (RSMLI) is specifically designed to be compact, reliable and adaptable to different

applications. In a symmetrical RSMLI configuration, all DC sources have the same voltage magnitude, whereas asymmetrical RSMLI has a variable ratio of DC source voltages as defined in Eq. [3-6].

For the case, let V_{DC1} is set to per unit voltage, 1 V_{pu}, and V_{DC2} and V_{DC3} follow the rules of progression, where k is the range of DC voltage from 1 to 3, and l starts from k to k+2.

$$V_{DC1} = 1 \quad (3)$$
$$V_{DC3} = l \quad (4)$$
$$V_{DC2} = k \quad (5)$$

where,

$k \in 1, 2, 3$

$l \in k, k+1, k+2$

Hence, the MLI output projection can be written as,

$$(V_{DC1}, V_{DC2}, V_{DC3}) = \left\{1, k, \sum_{l=k}^{k+2} l\right\} \quad (6)$$

Table 1 shows the projection of varying multilevel output in regard to different DC source combination in ARSMLI.

Table 1
Multilevel output scalability in terms of voltage per phase, V_{AN}, hierarchical voltage progression, total On-state switch, S_{ON} and projected voltage levels.

V_{AN} (V_{pu})	V_{DC1}, V_{DC2}, V_{DC3}	Total S_{ON}	Voltage level ($-\sum_1^{i=3} V_{DCi} \leq V_{AN} \leq \sum_1^{i=3} V_{DCi}$)
7	1 , 1 , 1	3	-3 -2 -1 0 1 2 3
9	1 , 1 , 2	4	-4 -3 -2 -1 0 1 2 3 4
11	1 , 1 , 3	5	-5 -4 -3 -2 -1 0 1 2 3 4 5
11	1 , 2 , 2	5	-5 -4 -3 -2 -1 0 1 2 3 4 5
13	1 , 2 , 3	6	-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
15	1 , 2 , 4	5	-7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7
15	1 , 3 , 3	5	-7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7
15	1 , 3 , 4	5	-8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8
19	1 , 3 , 5	5	-9 -8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9

While the ARSMLI configuration can be used with a variety of DC source combinations, including heterogeneous progression and numerical sequence progression, this study focuses on binary and trinary DC source progressions for their capacity to provide higher multilevel output voltages. As a result, the proposed inverter uses ARSMLI to synthesise different output levels by using the same switch counts and circuit designs. Although both 15-level and 19-level ARSMLIs share the foundational switching patterns, the output levels differ due to the distinct DC source progression applied. Figure 4 shows the switching sequence for the 15-level ARSMLI, employing a binary DC source progression (1:2:4), while, Figure 5 shows the extended sequence for the 19-level ARSMLI using a trinary DC source progression (1:3:5). The switching mode for these configurations are tabulated in Table 2 and Table 3.

Table 2
Switching pattern for 15-level ARSMLI with (1 ,2 ,4) voltage progression.

Switching Sequence										MLI Output
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o
0	1	1	0	0	1	1	0	1	0	V_7
0	1	1	0	1	0	1	0	1	0	V_6
0	1	0	1	0	1	1	0	1	0	V_5
0	1	0	1	0	1	0	1	1	0	V_4
0	1	0	1	1	0	0	1	1	0	V_3
0	1	1	0	1	0	1	0	0	1	V_2
0	1	0	1	0	1	1	0	0	1	V_1
0	1	0	1	0	1	0	1	0	1	**0**
1	0	1	0	1	0	0	1	1	0	$-V_1$
1	0	0	1	0	1	0	1	1	0	$-V_2$
1	0	1	0	0	1	1	0	0	1	$-V_3$
1	0	1	0	1	0	1	0	0	1	$-V_4$
1	0	1	0	1	0	0	1	0	1	$-V_5$
1	0	0	1	0	1	0	1	0	1	$-V_6$
1	0	0	1	1	0	0	1	0	1	$-V_7$

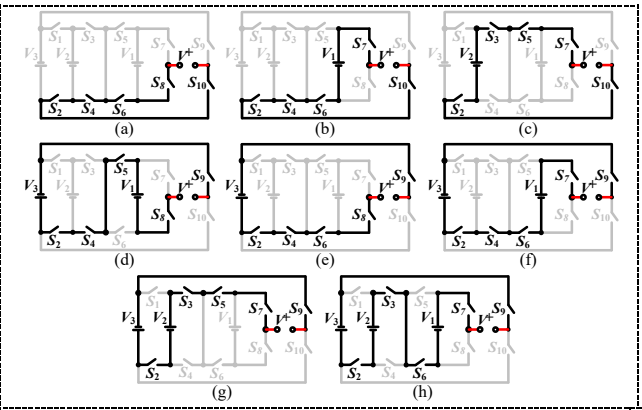

Fig. 4. Operating modes for 15-level ARSMLI, positive level output, (a) 0V, (b) 1V, (c) 2V, (d) 3V, (e) 4V, (f) 5V, (g) 6V, and (h) 7V

Table 3
Switching pattern for 19-level ARSMLI with (1 ,3 ,5) voltage progression.

Switching Sequence										MLI Output
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o
0	1	1	0	0	1	1	0	1	0	V_9
0	1	1	0	1	0	1	0	1	0	V_8
0	1	1	0	1	0	0	1	1	0	V_7
0	1	0	1	0	1	1	0	1	0	V_6
0	1	0	1	0	1	0	1	1	0	V_5
0	1	0	1	1	0	0	1	1	0	V_4
0	1	1	0	1	0	1	0	0	1	V_3
0	1	1	0	1	0	0	1	0	1	V_2
0	1	0	1	0	1	1	0	0	1	V_1
0	1	0	1	0	1	0	1	0	1	**0**
1	0	1	0	1	0	0	1	1	0	$-V_1$
1	0	0	1	0	1	1	0	1	0	$-V_2$
1	0	0	1	0	1	1	0	0	1	$-V_3$
1	0	0	1	1	0	0	1	1	0	$-V_4$
1	0	1	0	1	0	1	0	0	1	$-V_5$
1	0	1	0	1	0	0	1	0	1	$-V_6$
1	0	0	1	0	1	1	0	0	1	$-V_7$
1	0	0	1	0	1	0	1	0	1	$-V_8$
1	0	0	1	1	0	0	1	0	1	$-V_9$

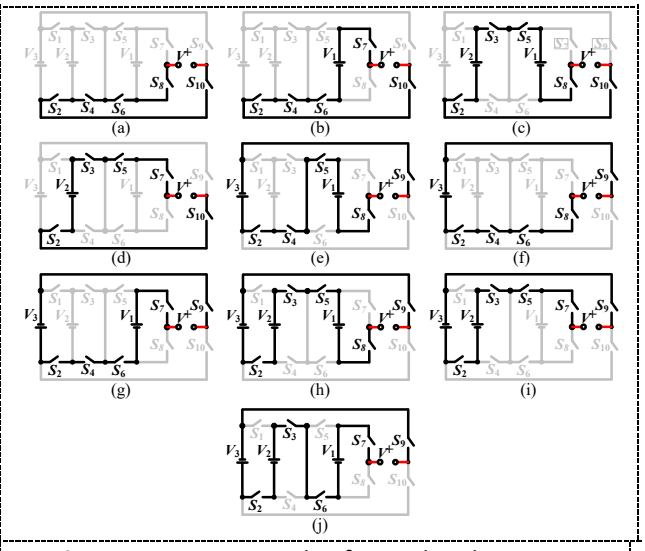

Fig. 5. Operating modes for 19-level ARSMLI, positive level output, (a) 0V, (b) 1V, (c) 2V, (d) 3V, (e) 4V, (f) 5V, (g) 6V, (h) 7V, (i) 8V and (j) 9V

MODE for the 15-level output:

i. **Zero Level:** Switches S_2, S_4, S_6, S_8 and S_{10} are turned-On, allowing current flow without supplying voltage to the load.
ii. **Level 1:** Switch S_7 connects the positive terminal of V_1 to the load, while switches S_2, S_4, S_6 and S_{10} complete the circuit by connecting the negative terminal of the DC source to supply V_1 to the load.
iii. **Level 2:** Switches S_3, S_5 and S_7 connect the positive terminal of V_2 to the load, with switches S_2 and S_{10} completing the circuit, delivering V_2 to the load.
iv. **Level 3:** Switch S_8 connects the negative terminal of V_1 to the load and switch S_9 connects the negative terminal of V_3 to the load. Switches S_2, S_4 and S_5 create a series connection of V_1 and V_3 supplying a differential voltage to the load.

v. **Level 4:** Switch S_9 connects the positive terminal of V_3 to the load, while switches S_2, S_4, S_6 and S_8 complete the circuit by connecting the negative terminal of the DC source to supply V_3 to the load.
vi. **Level 5:** Switch S_7 connects the negative terminal of V_1 to the load and switch S_9 connects the negative terminal of V_3 to the load. Switches S_2, S_4 and S_6 form a DC-link between V_1 and V_3. This configuration generates a desired differential voltage for the load.
vii. **Level 6:** Switches S_3, S_5 and S_7 connect the positive terminal of V_2 to the load, while switch S_2 establish a DC-link connection for V_2 and V_3. Switch S_9 connects the negative terminal of V_3 to the load, completing the circuit.
viii. **Level 7:** Switch S_7 connects the positive terminal of V_1 to the load. Switches S_3 and S_6 create a DC-link between V_1 and V_2 and switch S_2 forms a DC-link for V_2 and V_3. Switch S_9 connects the negative terminal of V_3 to the load. This setup combines all three DC sources to achieve the highest level MLI.

These switching configurations define the positive level outputs of the proposed ARSMLI. For negative level outputs, the DC Sources' polarity with respect to the load is reversed. Combining both positive and negative level output results in the 15-level output exhibiting incremental step characteristics.

In the 19-level output, the switching pattern is extended with additional modes, as shown by the inclusion of Level 2 in Figure 5(c) and Level 7 in Figure 5(h).

Additional MODE in 19-level output:

i. **Level 2:** Switch S_8 connects the negative terminal of V_1 to the load and switches S_2 and S_{10} connects the negative terminal of V_2 to the load. Switches S_3 and S_5 form a DC-link between V_1 and V_2, delivering a differential voltage to the load.
ii. **Level 7:** Switch S_8 connects the negative terminal of V_1 to the load and switch S_9 connects the negative terminal of V_3 to the load. Switches S_3 and S_5 create a DC-link between V_1 and V_2 and switch S_2 forms a DC-link for V_2 and V_3.

The generation of intermediate voltage levels representing the progression of trinary DC source creates these additional modes. These switching configurations produce a higher level MLI output and improves the inverter output resolution.

4. Performance Analysis

In this section presents the performance of 15-level and 19-level ARSMLI in a three-phase application setting. The performance of ARSMLI varies significantly depending on the modulation strategies and also the number of inverter output levels. The ARSMLI is analysed by utilizing SHEPWM and MCPWM PD, POD, APOD. In MCPWM, the same modulation index is applied and carrier frequency is maintained at 5000 Hz. The simulation parameters of the 15-level ARSMLI were studied at a load of R = 1000 Ω with the DC source ratio is set to multiply by 100 V.

Figure 6 and 8 illustrated the line-to-line output voltage, V_{AB} and THD performance for SHEPWM modulation at three different modulation indices of 0.6, 0.8, and 1.0 highlighting how varying the modulation index affects the output quality and harmonic performance for 15-level and 19-level inverter setup respectively. While, Figure 7 and 9 illustrated the line-to-line output voltage, V_{AB} and

THD performance for MCPWM modulation at three different disposition methods; PD, POD, and APOD for 15-level and 19-level inverter setup respectively.

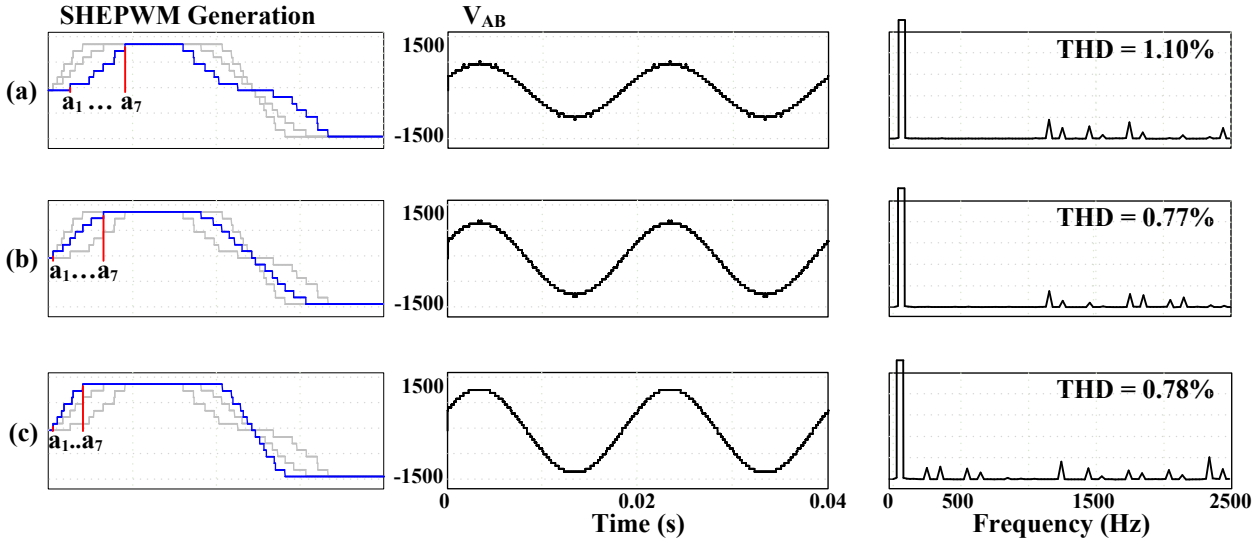

Fig. 6. SHEPWM signal generation, line-to-line output voltage and total harmonic distortion for each varying modulation technique applied to 15-level ARSMLI; (a) M_i = 0.6, (b) M_i = 0.8, and (c) M_i = 1.0.

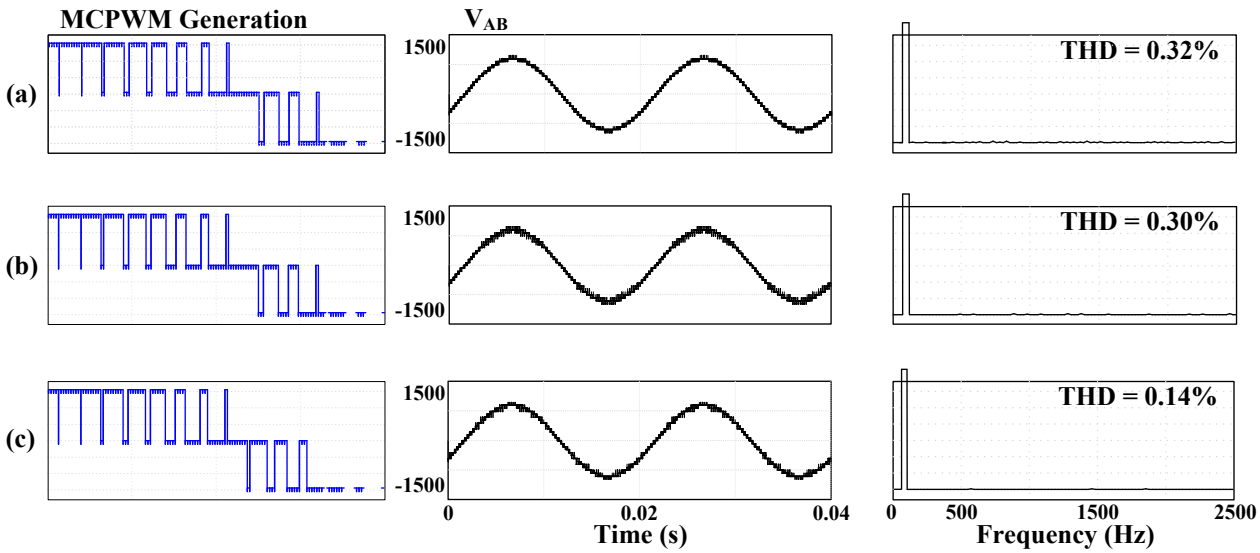

Fig. 7. MCPWM signal generation, line-to-line output voltage and total harmonic distortion for each high frequency modulation technique applied to 15-level ARSMLI; (a) PD, (b) POD, and (c) APOD.

For a 15-level MLI, SHEPWM operation with a modulation index, M_i of 0.8 rather have better THD performance of 0.77% as shown in Figure 6. In compared to other SHEPWM modulation settings, such as M_i 0.6 and 1.0, result in higher THD due to less effective harmonic elimination, lower or higher fundamental voltage value due to under-modulation and over-modulation, and also the increased of output voltage distortion. As for MCPWM, the comparison in Figure 7 clearly indicates that APOD has the lowest THD at 0.14%, proving its ability to produce a clean output waveform by removing undesired harmonics throughout a wide frequency range. In comparison, POD MCPWM has a THD of 0.3%, while PD MCPWM has slightly higher THD of 0.32%. These findings demonstrate the effectiveness of phase opposition strategies in minimizing the undesired harmonics.

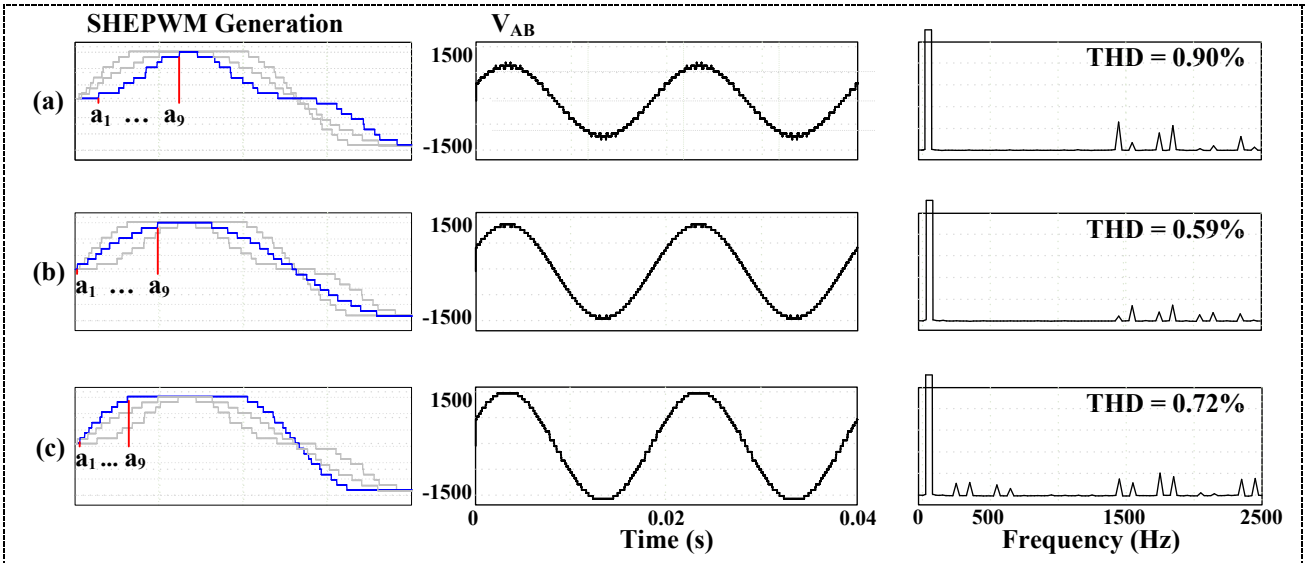

Fig. 8. SHEPWM signal generation, line-to-line output voltage and total harmonic distortion for each varying modulation technique applied to 19-level ARSMLI; (a) M_i = 0.6, (b) M_i = 0.8, and (c) M_i = 1.0.

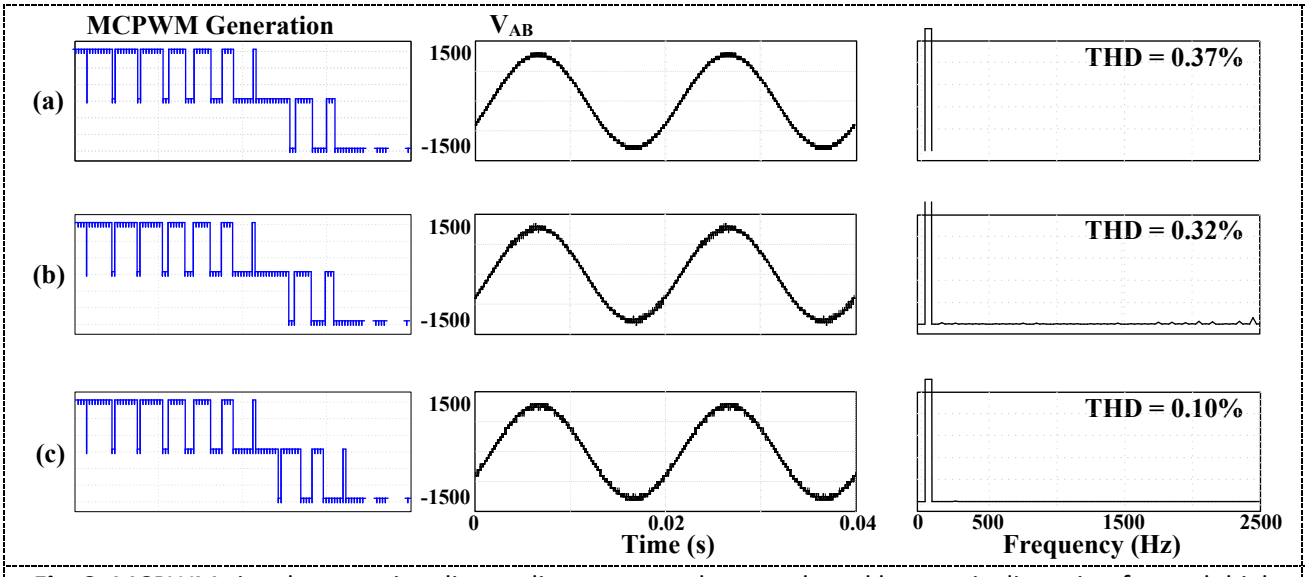

Fig. 9. MCPWM signal generation, line-to-line output voltage and total harmonic distortion for each high frequency modulation technique applied to 19-level ARSMLI; (a) PD, (b) POD, and (c) APOD.

SHEPWM's performance increases with the output increased to 19-levels, with a M_i of 0.8 resulting in a THD of 0.6%, but it still inadequate to reach the low THD produced by APOD MCPWM. These can be observed in Figure 8. Again, at higher modulation indices, SHEPWM exhibits an uncertain rise in THD, indicating difficulties in managing over-modulation. As for the MCPWM in Figure 9, the similar patterns were observed when APOD MCPWM modulation was applied to a 19-level MLI. This method achieved the lowest THD of 0.1%, demonstrating its better harmonic reduction capabilities even at higher levels. POD MCPWM has a slight increase with THD of 0.32%, whereas PD MCPWM's THD rises slightly to 0.37%, showing the performance more or less effecting by the high frequency switching as the number of levels grows.

Comparing modulation techniques for 15-level and 19-level ARSMLI module, THD reductions were observed with an increased level of MLI output, but a more significant difference was shown by the choice of the modulation technique itself. Therefore, for MLIs that require the best power quality, APOD MCPWM is the most effective approach, delivering the lowest THD and high performance

across all output levels. POD MCPWM also performs well, achieving a balance of harmonic reduction and simplicity in the phase shift implementation. PD MCPWM, while easier to be implemented, has disadvantages as the MLI levels increase. SHEPWM, while beneficial for specific undesired harmonic removal, but typically produces more THD than MCPWM approaches. As a result, APOD MCPWM is ideal for applications that require high power quality, such as grid-connected systems, whereas SHEPWM is better suited for specific harmonic management requirements where the output quality is not the main priority.

5. Conclusions

This paper focuses on comparing the performance of the proposed ARSMLI inverter topology in two different switching configurations: 15-level and 19-level, employing two different modulation techniques: SHEPWM and MCPWM modulation techniques. The goal is to provide a summative analysis that can provide an insight into determining the effective modulation strategies for power converter applications, especially in reduced-switch MLI. In terms of inverter configurations, the transition from binary to trinary DC source progression introduces more intermediate levels, allowing better output quality, however, requires switching management to avoid faulty operation and to maintain the inverter output operation. Meanwhile, the modulation comparative study shows APOD MCPWM is the most effective method for removing undesired harmonics in inverter, hence, high-quality output is obtained. This is important, especially in medium to high power application scenarios where efficiency is a significant consideration. In summary, although SHEPWM and MCPWM are both practical for the proposed ARSMLI configuration, the selection consideration of these modulation approaches is determined by the complexity of the modulation technique implementation and the sensitivity of output quality for power conversion applications. SHEPWM excels in removing the most significant undesired harmonic using low switching, hence low switching loss and easy implementation. However, its fixed switching angle condition limits its flexibility from responding to dynamic changes in load or sudden alteration in inverter application conditions. In contrast, MCPWM provides excellent performance in removing undesired harmonic but suffers from higher switching losses, increased EMI and greater stress on the switching device due to the fast-switching rate. Thus, the hardware can be bulkier and more complex. As to conclude, the understanding of these trade-offs is essential to choose the appropriate modulation technique based on the needs and constraints of the specific power converter system.

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