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Examining the Impact of Negative Bias Temperature Instability on the Performance of Domino Logic Circuits

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ABSTRACT

Negative Bias Temperature Instability (NBTI) poses a notable reliability concern in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), causing an aging effect that alters threshold voltage and reduces drain current. This effect holds particular significance in sub-micrometre CMOS circuitry. This study focuses on assessing NBTI's impact on domino logic circuits, exploring various NBTI defect mechanisms like interface trap (N_{it}) and oxide trap (N_{ot}). Evaluations extend to NOR and NAND domino logic circuits, analysing delay and average power to gauge NBTI effects. The study employs the Predictive Technology Model (PTM) based on 32nm technology, coupled with the MOSRA model, to illustrate circuit dependability. Simulations involve varied stress temperatures, revealing a proportional degradation in delay with increasing temperature. Specifically, when N_{it} serves as the sole defect mechanism, the time exponent stands at 0.25, whereas N_{it} and N_{ot} together reduce this exponent to 0.167. Higher stress temperatures correlate with increased delay, reduced average power, and a shift in threshold voltage towards higher values over prolonged stress durations.

1. Introduction

Negative Bias Temperature Instability (NBTI) has emerged as a primary concern for CMOS circuit reliability in nano-scale designs. This phenomenon is frequently observed in p-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) [1] when subjected to negative gate voltages at elevated temperatures. NBTI typically occurs during the PMOS transistor's operation under negative bias (VGS = -VDD) at high temperatures [1,2] contributing to the shifting of its threshold voltage (V_{th}) over time [3]. This alteration in V_{th} can notably increase PMOS delay, thereby degrading circuit speed and shortening its operational lifespan [4,5]. Mitigating the impact of NBTI is crucial for enhancing

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circuit performance. Currently, study related to reliability in electronic system [6] is conducted to study on the validity and capability of electronic system. Many tools include TCAD [7] and other simulation tools is seen as important method in developing such study. Many electronic systems that include low power applications are researched by the use of simulation tool thus enable studies in advanced and intelligent devices in our daily lives [8].

The study of NBTI revolves around the rate-diffusion model (R-D model) [2,9-11]. In the PMOS transistor, NBTI arises from the attraction of positive holes to the Si/SiO_2 interface, weakening the Si-H bonding until breakage occurs, illustrated in Figure 1 [12,13]. This breakdown leads to continual hydrogen diffusion, creating traps within the Silicon substrate's oxide during oxidation. Consequently, the generation of H or H2 molecules prompts an increase in the transistor's V_{th} [14].

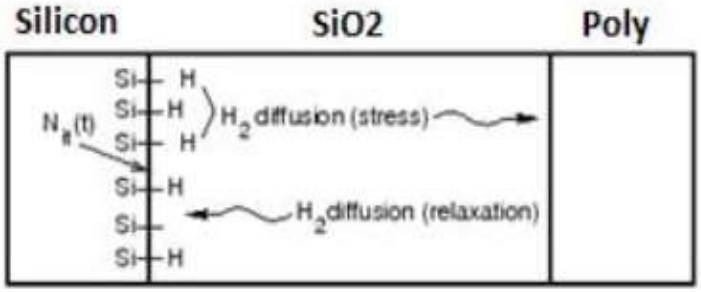


Fig. 1. Schematic description of the R-D model [12,13]

The presence of interface traps persists as H or H_2 molecules diffuse away, causing a shift in V_{th} and subsequent degradation in drain current [15]. Recent advancements in NBTI measurement setups have revealed the role of oxide traps (N_{ot}) [16] in contributing to this degradation. The characterization results of NBTI are contingent upon the measurement delay following stress interruption, influenced by the recovery effect [17]. To ensure accuracy, it is advantageous to conduct measurements promptly after stress removal, particularly when stress and measurement occur at the same elevated temperature [18]. This approach maximizes reliability in assessing NBTI behaviour. While the underlying physical mechanism is subject to ongoing debate, there is widespread acceptance that the traps present within the dielectric primarily contribute to BTI degradation [19]. Discrepancies in charge between the interface and oxide induce variations in threshold voltage. The threshold voltage shift can be calculated as Eq. (1) that follows [16]:

$$\Delta V_{th} = -\frac{\Delta Q_{ox}(t)+\Delta Q_{it}(t)}{C_{ox}} \quad (1)$$

As CMOS technology continues to scale down to the nanoscale, the prominence of reliability issues intensifies. Among the foremost challenges in fortifying the reliability of very-large-scale-integrated (VLSI) circuits are the aging effects, notably the NBTI [4,20-22]. NBTI in PMOS transistors has become a critical concern in modern digital circuit design. This project investigates NBTI's impact on the primary performance of N-type domino NAND and NOR gates, commonly used in high-performance circuit designs due to their reduced transistor count and heightened operational speed [5]. The primary function of domino logic circuits is to expedite circuit operations. Domino logic circuits are widely utilized in high-performance microprocessors owing to the superior speed and space efficiency offered by dynamic CMOS circuits compared to static CMOS ones. The high-speed performance of domino logic circuits is primarily attributed to their lower noise margins compared to static gate [23]. Numerous domino logic configurations have been introduced in academic

literature to address challenges and enhance performance. These design adaptations in domino logic primarily focus on minimizing leakage current, decreasing both static and dynamic power consumption, mitigating charge sharing issues, improving operating speed and ensuring robustness. These enhancements are typically achieved through more efficient keeper control mechanisms, restructuring the pull-down network, or minimizing redundant output switching transitions [24].

This paper delves into the NBTI defect mechanisms' effects on the delay and power of NOR and NAND domino logic circuits, alongside the threshold voltage discrepancies in PMOS, all under varied temperature conditions. High temperatures significantly affect delay, and distinct mechanisms result in varying levels of NBTI degradation.

2. Simulation Details

2.1 Simulation Design Flow

Figure 2 depicts the flowchart detailing the Hewlett Simulation Program with Integrated Circuit Emphasis (HSPICE) simulation sequence [25]. The process initiates with the generation of the netlist file, "nor.sp," outlining the entire schematic of the domino NOR logic circuit. CosmoScope facilitates the observation of output waveforms, generated and plotted based on the data stored in the .tr# file, encompassing transient analysis results.

Figure 3 illustrates the MOS Reliability Analysis (MOSRA) process involved in HSPICE MOSRA reliability simulations [25-27]. This MOSRA simulation comprises two distinct phases: POST-stress and PRE-stress. The "Fresh" simulation denotes the PRE-stress phase, responsible for calculating the electrical stress experienced by selected MOSFETs within the circuit, utilizing the MOSRA model. Conversely, the post-stress phase occurs after the PRE-stress phase. Its purpose is to simulate the degradation effects on circuit performance, using information gleaned from the preceding simulation. This phase culminates in presenting the circuit's performance at the end of its lifetime (EOL).

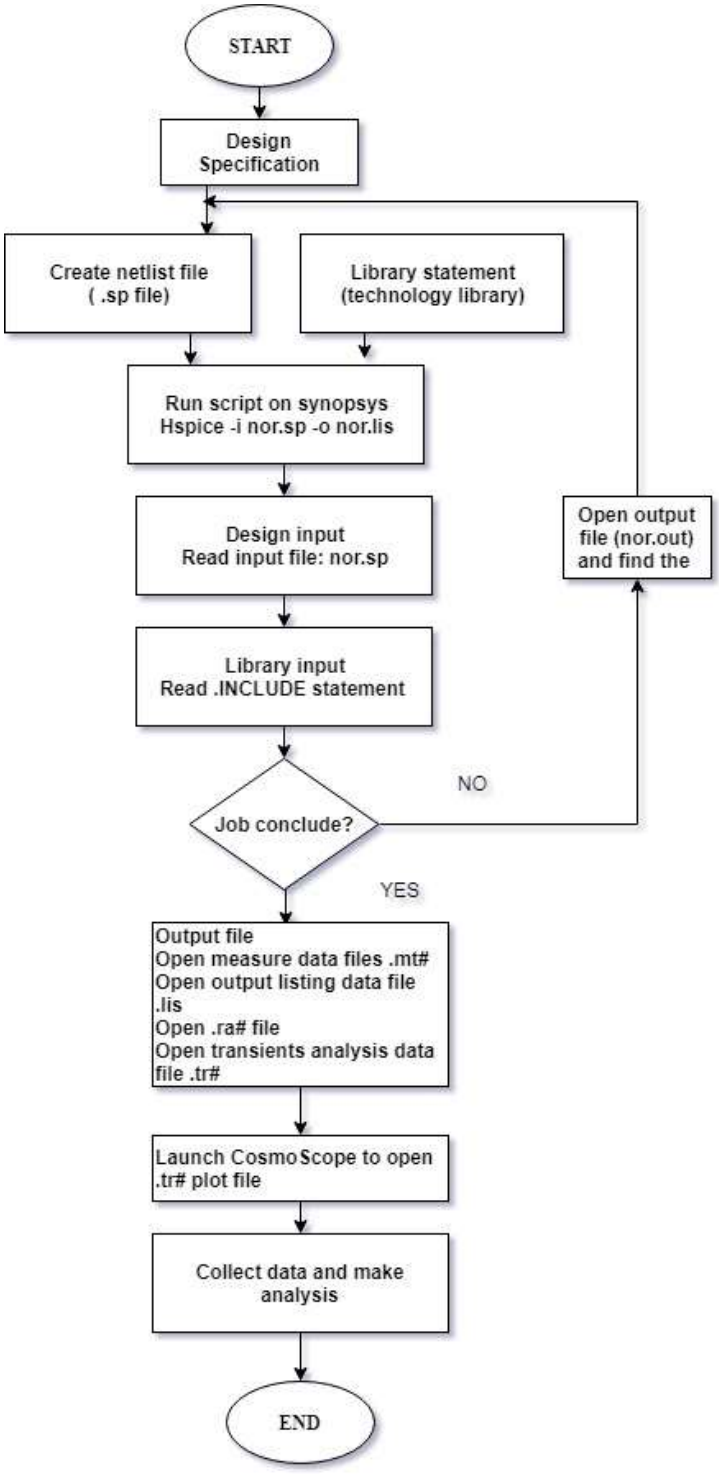


Fig. 2. Flowchart HSPICE simulation

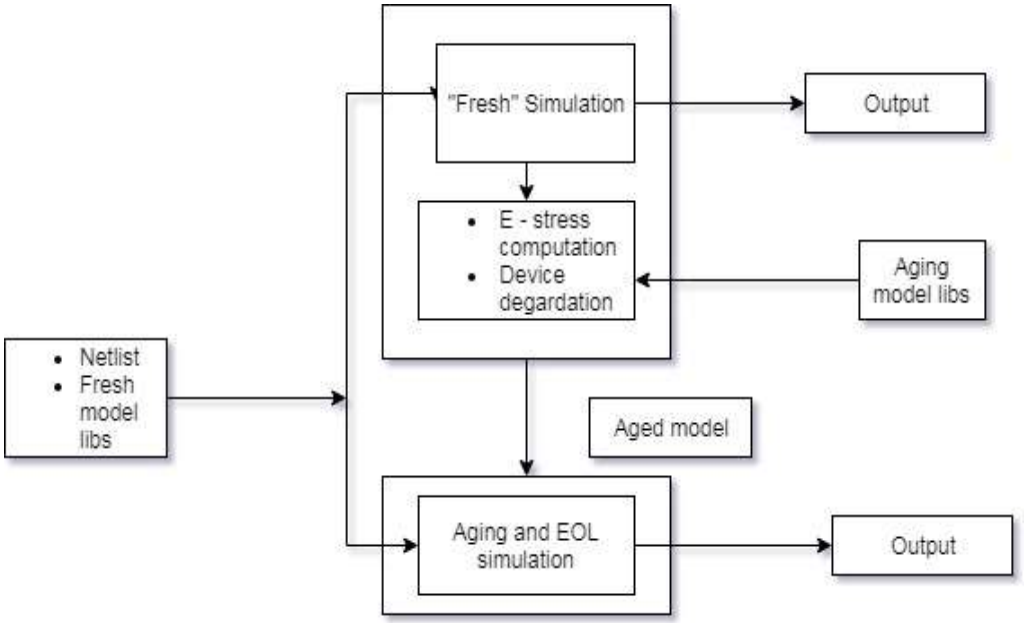
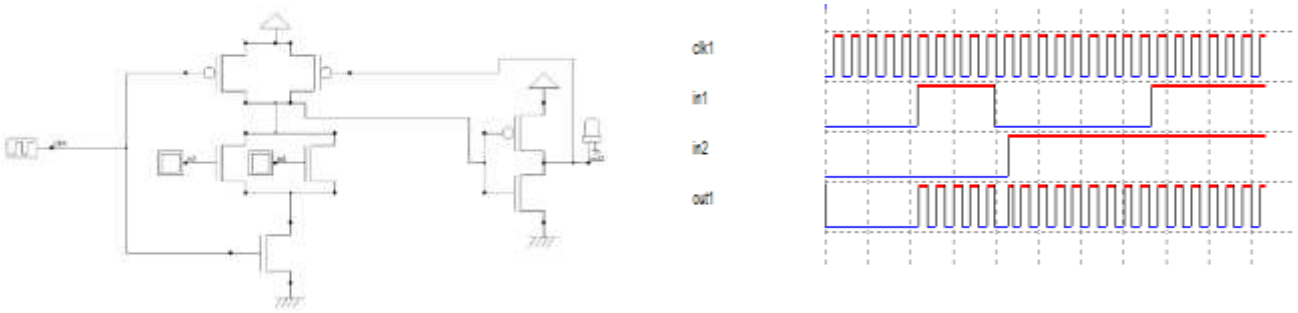


Fig. 3. Flowchart HSPICE simulation

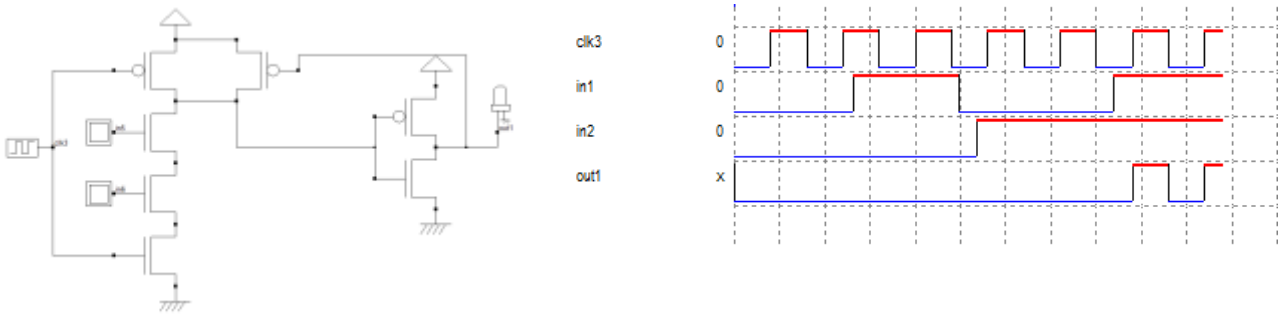
2.2 The Circuit

Figure 4(a) and 4(b) display the schematic diagram and output of the NOR Domino logic respectively, while Figure 5(a) and 5(b) depicts the schematic diagram and output of the NAND Domino logic. Both schematic diagrams are created through Design Schematic Editor Tool (DSCH) software.



(a) (b)

Fig. 4. NOR Domino (a) Schematic diagram (b) Timing diagram



(a) (b)

Fig. 5. NAND Domino (a) Schematic diagram (b) Timing diagram

Figure 6 illustrates the Propagation graph utilized for computing the delay values from the circuits proposed in this paper. The delay values are obtained by considering the 50% point between input and output crossings [28].

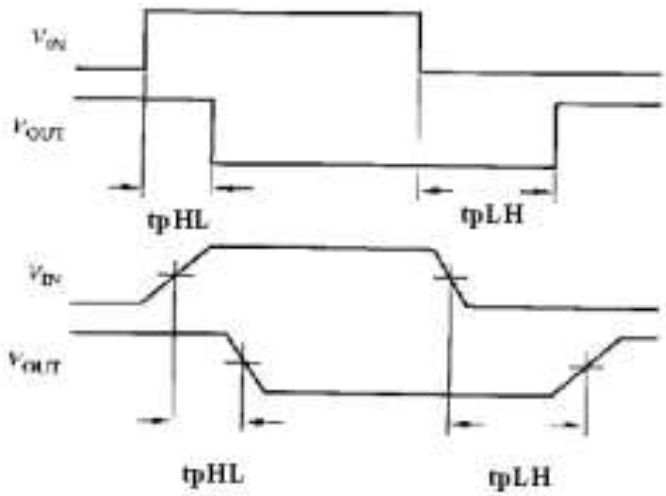


Fig. 6. Propagation delay graph

The propagation delay (t_p) in the circuit represents the duration required for a signal to travel from the input to the output. This delay plays a crucial role in determining the circuit's speed. During the evaluation phase of the circuit, the delay is assessed. Inputs are introduced to the circuit, and the output is recorded. To compute the delay, the superimposition of any one of the input signals onto the output signal is performed. The calculation is carried out as in Eq. (2) that follows [29]:

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} \tag{2}$$

2.3 Simulation Condition

In this study, three distinct temperatures—25°C, 75°C, and 125°C—were utilized to compare circuit performance using the 32nm Predictive Technology Model (PTM) [30]. These temperatures align with the operational range of the 32nm technology [31]. Throughout simulations, the W/L ratio remains constant.

The investigation delves into various defective mechanisms, notably N_{it} and the combined effects of N_{it} and N_{ot}. Table 1 categorizes dynamic NBTI into three distinct commands [25]. The first command illustrates normal dynamic NBTI behaviour, while the second command demonstrates a longer recovery time for the dynamic NBTI simulation compared to the stress duration. The third command portrays a scenario where the circuit experiences normal NBTI dynamics in the initial half cycle, followed by a recovery period in the subsequent half cycle, all within a 1-second timeframe [26].

Table 1
Different measurement setup for HSPICE reliability simulation

Measurement Setup	Commands
Command 1	.MOSRA Reltotaltime = 3.154e+8 RelStep = 3.154e+7 .Tran 0.01n 4ns
Command 2	.MOSRA Reltotaltime = 3.154e+8 RelStep = 3.154e+7 +AgingStart=10ns AgingStop = 100ms +AgingPeriod=1s .Tran 0.01n 4ns
Command 3	.MOSRA Reltotaltime = 3.154e+8 RelStep = 3.154e+7 +AgingPeriod=1s Agingwidth=0.5s .Tran 0.01n 4ns

3. Simulation Results and Discussion

3.1 Simulation Verification

Figure 7 presents the outcomes of threshold voltage shifts resulting from NBTI degradation at a temperature of 125°C. Two distinct NBTI mechanisms, N_{it} and a combination of N_{it} and N_{ot}, were employed in simulations to validate the integration of the PTM model with the MOSRA HSPICE model. In Figure 7(a), N_{it} showcased a more substantial contribution to threshold voltage shifts compared to the combination of N_{it} and N_{ot}. N_{it} induces permanent degradation, whereas N_{ot} demonstrates a recoverable effect. Simulations indicated that while N_{it}-only degradation escalates, combining N_{ot} with N_{it} initiates a recovery process, ultimately confirming N_{it}'s higher degradation impact [16,26]. Figure 7(b) illustrates Simulation condition 1, S1 having higher values than Simulations condition 3, S3 and Simulations condition 2, S2. S1 represents standard dynamic NBTI with the longest stress duration. In the second condition, the recovery time for dynamic NBTI simulation surpasses the stress duration, explaining its lower values. S3 illustrates a scenario where the circuit experiences normal NBTI in the initial half cycle followed by a recovery period in the subsequent half cycle within a 1-second timeframe [9].

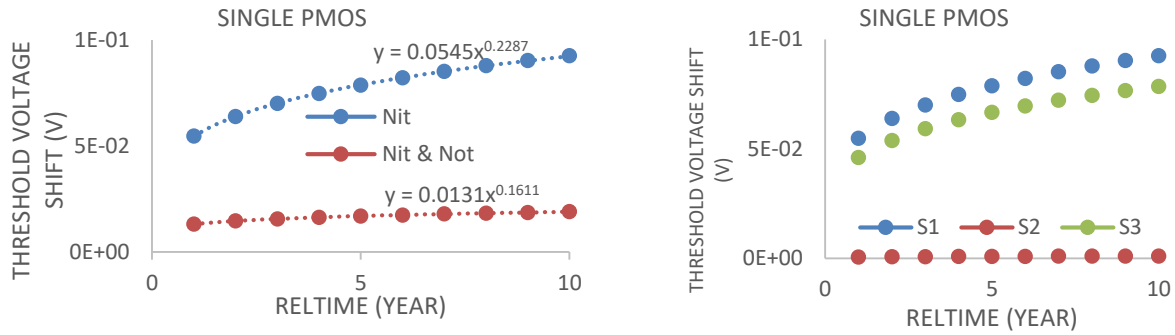


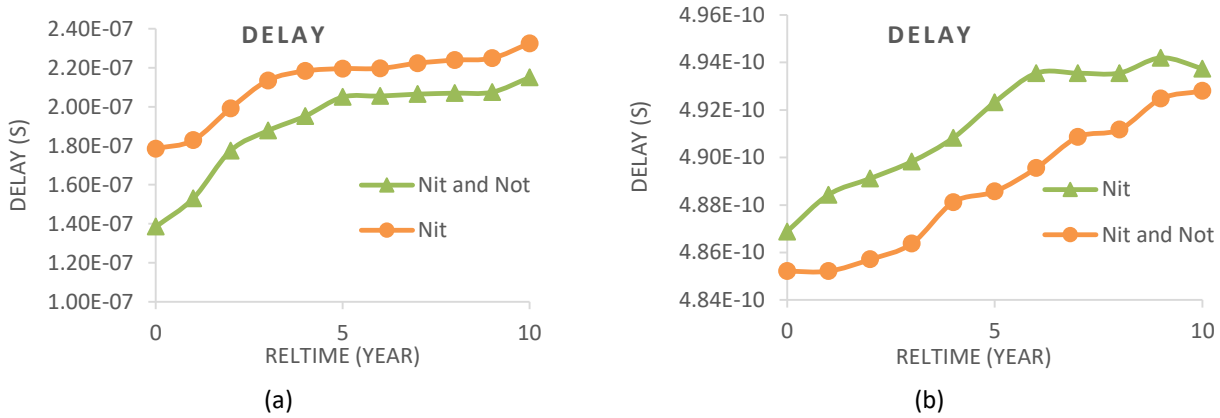
Fig. 7. (a) Defect mechanism (b) Different simulation condition

3.2 Delay Degradation

Figures 8 - 11 present the outcomes illustrating delay degradation resulting from the NBTI effect. The study primarily delves into the impact of diverse defect mechanisms, various simulation conditions, and distinct stress temperatures on domino circuits. Delay calculation involves the formula in Eq. (3) [32]:

$$Tp = (Tplh + Tphl)/2 \quad (3)$$

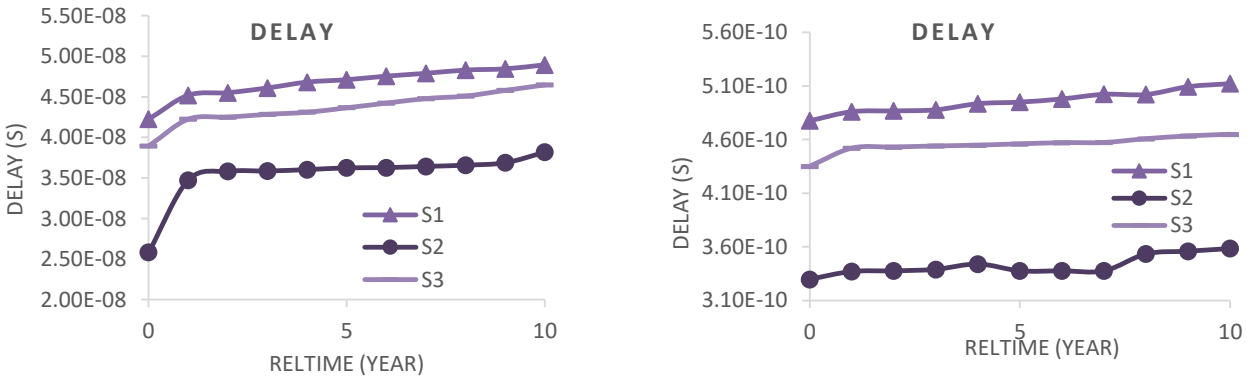
Under Condition 1 and at a temperature of T = 125°C, specific transistor conditions, as depicted in Figure 8, demonstrate delay results measured under precise conditions. Analysis of N_{it} and the combined N_{it} and N_{ot} mechanisms reveal an incremental delay from the pre-stress (fresh) state [33] to the ten-year mark, albeit with a minimal widening gap. When applied to both circuits (a) and (b), the N_{it} mechanism showcases the most significant delay degradation compared to the combination of both mechanisms over the ten-year period [25,34].



(a) (b)

Fig. 8. (a) NAND domino circuit (b) NOR domino circuit

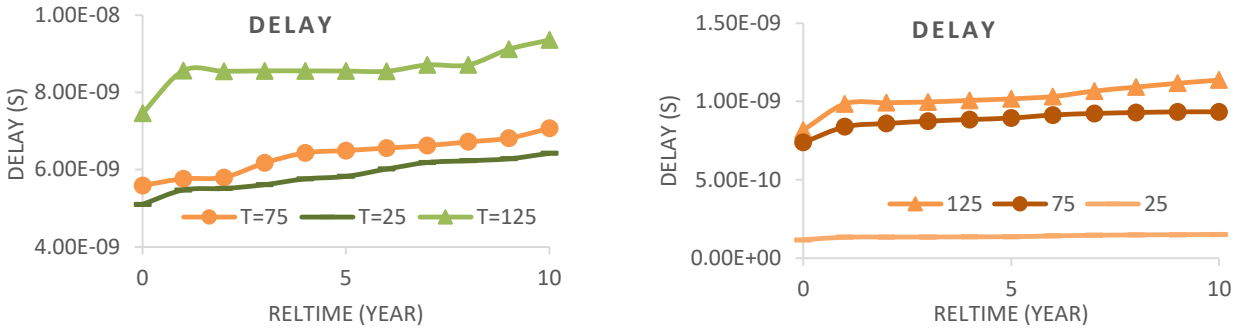
Under various simulation conditions depicted in Figure 9, it is observed that simulation 1 exhibits the most significant delay degradation, followed by simulations 3 and 2, owing to the N_{it} defect mechanism at a constant temperature of 125°C. The reliability degradation in simulation 1 is assessed at intervals of 1e+8 seconds until reaching a total duration of 1e+9 seconds. Stress values are determined during the pre-stress simulation within the initial 100ns of inputs [35].



(a) (b)

Fig. 9. (a) NAND domino circuit (b) NOR domino circuit

The escalation of temperature formerly contributed to delay degradation. As depicted in Figure 10, there's a clear correlation indicating that as the temperature rises, the delay also experiences an increase [31].



(a) (b)

Fig. 10. (a) NAND domino circuit (b) NOR domino circuit

Figure 11 illustrates the impact of NBTI on the Domino Logic circuit under examination in this study. Specifically, when employing the N_{it} defect mechanism at condition 1 and a temperature of 125°C, the results reveal a significant difference in delay degradation between the NAND domino logic circuit and the NOR domino logic circuit. The delay degradation for the NOR domino circuit is recorded at 15.91%, notably higher than that of the NAND domino circuit at 6.49%, as demonstrated in Figure 12.

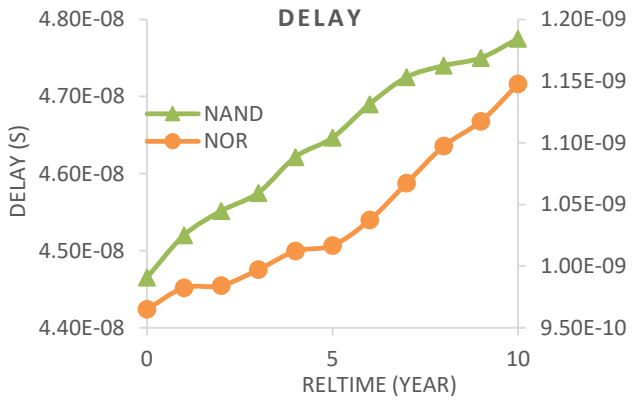


Fig. 11. NAND domino circuit comparison with NOR domino circuit for delay degradation

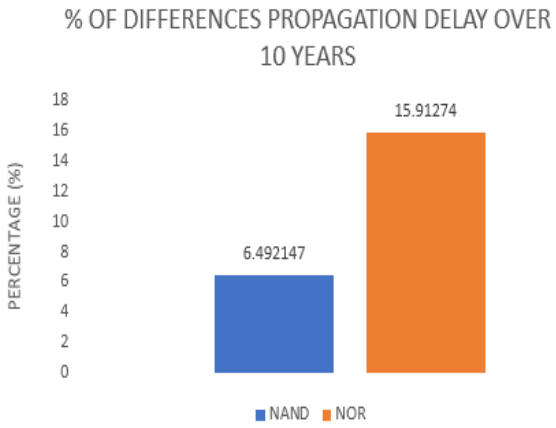
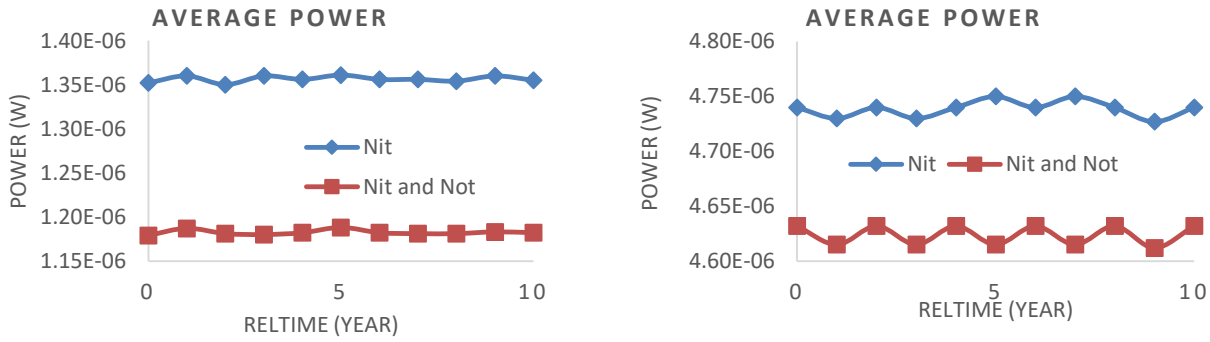


Fig. 12. NAND domino circuit comparison with NOR domino circuit for delay degradation

3.3 Average Power

The study aimed to examine the impact of varied defect mechanisms, simulation conditions, and stress temperatures on the average power consumption of the domino circuit during operation.

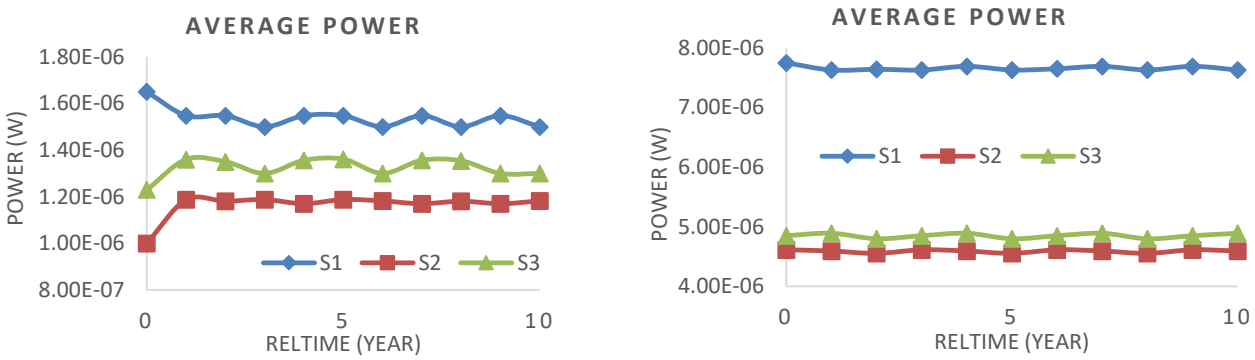
Analysis of the average power consumption concerning different defect mechanisms reveals that N_{it} exhibits the highest average power consumption for both the NOR and NAND domino logic circuits, illustrated in Figure 13. This observation suggests that the Ni_t and N_{ot} mechanisms yield comparatively lower NBTI effects when contrasted with other mechanisms [34].



(a) (b)

Fig. 13. (a) NAND domino circuit (b) NOR domino circuit

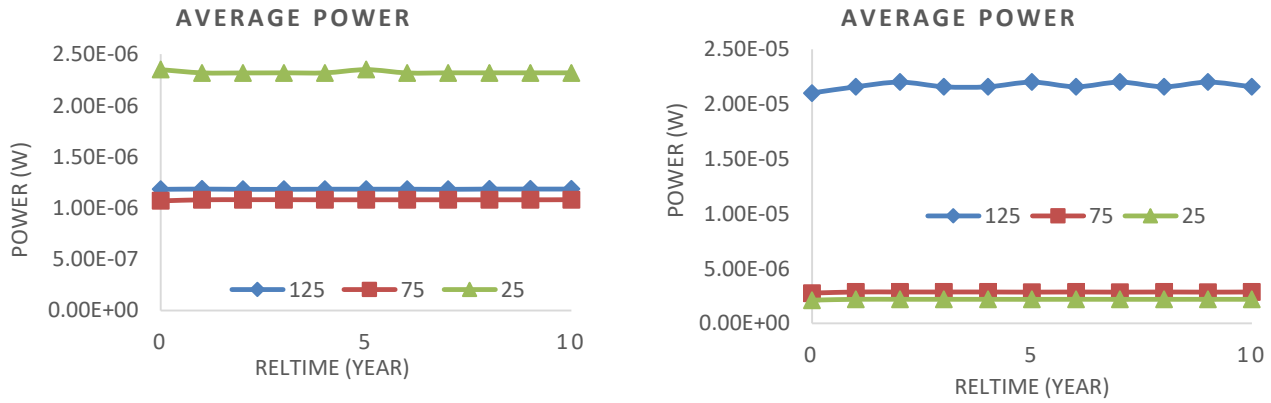
The investigation scrutinized the average power across varying aging periods under three distinct simulation conditions. Notably, simulation conditions 3 and 2 manifest the lowest average power, whereas simulation condition 1 exhibits the highest average power, as depicted in Figure 14. This observation underscores the direct correlation between average power and the propagation delay, elucidated in Part B.



(a) (b)

Fig. 14. (a) NAND domino circuit (b) NOR domino circuit

As shown in Figure 15(a), the NAND domino circuit has higher power consumption operated at normal temperature. However, subjected to stress temperature condition, higher temperature shows more average power consumption. Increasing the circuit's temperature correlates with a subsequent rise in average power consumption, as depicted in Figure 15(b) for NOR domino logic circuits. The NOR domino circuit shows lowest average power at normal operating temperature.



(a) (b)

Fig. 15. (a) NAND domino circuit (b) NOR domino circuit

Figure 16 depicts the impact of NBTI on the Domino Logic circuit employed in this study. Specifically, utilizing the N_{it} defect mechanism under condition 1 at a temperature of 125°C, the results reveal that the NOR domino logic circuit exhibits a higher average power consumption compared to the NAND domino logic circuit.

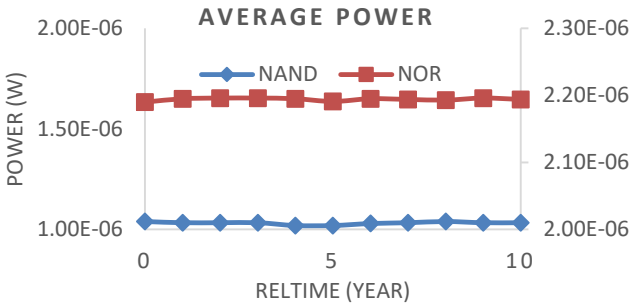


Fig. 16. Average power of the NOR domino circuit is higher than NAND domino circuit

4. Conclusions

This investigation underscores the critical consideration of aging effects, particularly NBTI, in digital circuit design. The choice of mechanisms demands meticulous understanding, given the distinct threshold voltage shifts observed across simulations using different NBTI mechanisms. Notably, when N_{it} operates as the singular defect mechanism, a more pronounced delay degradation is evident compared to scenarios involving a combination of N_{it} and N_{ot}. Moreover, escalating temperatures directly correlate with increased average power consumption and delay degradation. Simulation conditions highlight that simulation condition 1, characterized by the longest stress time, significantly contributes to the highest average power consumption and delay degradation in both circuits under scrutiny. These findings underscore the nuanced interplay between aging effects, defect mechanisms, temperature, and stress duration in shaping circuit performance, emphasizing their pivotal role in digital circuit design considerations.

Acknowledgements

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