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Design of a 100 Watt High Gain Cascaded Modified Boost Converter with Continuous Input Current

Mohd Nadzri Mamat[1,*], Dahaman Ishak[2], Suardi Kaharuddin[1], Mohamad Nazir Abdullah[1]

[1] School of Electrical of Electrical and Electronic Engineering, Universiti Sains Malaysia, Pulau Pinang, Malaysia
[2] Electrical Engineering Department, Prince Muhammad Bin Fahd University, Al Khobar, Saudi Arabia

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ABSTRACT

The conventional boost topology can be constructed to achieve high voltage gain by employing an extreme duty cycle, which can lead to inefficiencies, heightened voltage stresses, and instability. In order to address these challenges, this study introduces a high gain cascaded modified boost converter. This converter is specifically tailored for low voltage input sources necessitating high voltage amplification, such as those found in renewable energy systems. The design offers advantages including simplified switching control, high voltage gain, consistency across a broad duty cycle range, continuous input current, and scalability for achieving further gains. The paper elaborates on the operational principles, design considerations, and specifications of this proposed converter. Validation through Simulink simulations has demonstrated that the proposed design can effectively operate within the specified parameters, delivering a well-regulated output of 96 V and 1.04 A from a 12 V input source, with minimal output ripple of less than 0.4%.

1. Introduction

Utilizing renewable energy sources like solar panels, fuel cells, and wind turbines for energy production is a key focus in achieving a net zero solution. These sources typically generate low voltage levels suitable for low power applications. To maximize their benefits, the voltage needs to be increased to a higher level using a step up DC-DC converter. There are various studies on the design of these converters, which can be categorized into basic and advanced high gain topologies, as well as non-isolated and isolated topologies. Non-isolated topologies are commonly used in low to medium power applications due to their simplicity in design, control circuitry, and cost effectiveness compared to the more complex and expensive isolated topologies [1-3].

One of the commonly utilised configurations for voltage step up operations is the boost converter, which serves as a fundamental component known for its ability to increase voltage levels. However, conventional boost converters encounter limitations, particularly when confronted with the necessity for significantly higher voltage amplifications. Traditional designs require an extreme

* *Corresponding author.*
E-mail address: eenadzri@usm.my

duty cycle to achieve substantial gains, resulting in design instability and suboptimal performance. To overcome this challenge, numerous researchers [4-11] have restructured and enhanced the traditional boost converter design to develop high gain variants suitable for a range of medium to high power applications. A high gain boost converter can achieve notably elevated voltage amplifications while maintaining high efficiency and stability. Essentially, it elevates the input voltage to a significantly higher level at the output, while operating with a lower duty cycle for the same power requirement. In the era of renewable energies, where voltage escalation is crucial for effective power transmission, the necessity for high gain boost converters is paramount. The primary challenge in designing high gain boost converters lies in balancing the inherent trade-offs between efficiency, size, and complexity. As voltage levels rise, the stresses on converter components also increase, necessitating meticulous component selection and design considerations to optimize performance. The applications of high gain boost converters are diverse and extensive, encompassing sectors such as the automotive industry for hybrid and electric vehicles, online and offline smart grid systems, and high power portable instruments [12,13].

Numerous novel topologies and control methods have been developed in recent years to tackle the challenges associated with designing high gain boost converters. For instance, an improved gain quadratic boost converter was proposed in Subhani *et al*., [14], which incorporated a single switching control along with a voltage doubler feature to achieve a high voltage gain at medium duty cycle while maintaining continuous input current. Another approach Samat *et al*., [15] introduced a DC-DC multilevel scheme to enhance voltage gain, utilizing a four level synchronous modular multilevel configuration to reduce duty cycle and achieve high voltage gain, although requiring a more intricate switching strategy and a higher component count. Additionally, a three level converter with soft switching was devised in Taghavi *et al*., [16] to minimize input current ripple and voltage stresses across switches, necessitating precise timing for zero current switching. Furthermore, an alternative high gain boost converter employing a voltage lift technique was devised in Sanjeevikumar and Rajambal [17], employing a single switch to simplify the design, although requiring numerous inductors and capacitors to elevate the input voltage to the desired output level. Another topology Rajabi *et al*., [18] also utilizing the voltage lift technique necessitated two switches for circuit operation and resulted in reverse polarity at the output stage. Moreover, a modified quadratic boost converter was developed in Jana *et al*., [19] to enhance voltage gain beyond typical quadratic designs, incorporating a single switch along with additional diodes and capacitors, thereby requiring precise timing during its conduction period. An extended high gain boost converter utilizing a single switch was also introduced in Mansour *et al*., [20], capable of achieving high voltage gain at a moderate duty cycle and enabling cascading for even higher voltage gain. An isolated converter derived from Zeta topology was constructed in Inampudi *et al*., [21] that featured high voltage gain and low switching losses. In Mamat *et al*., [22], a modified SEPIC-boost converter was presented, featuring a high voltage gain design with regulated output at the output stage, and utilizing a single switch to simplify the switching strategy. Lastly, a modified four leg interleaved converter was presented in Veerendra et al., [23] capable of producing a high voltage gain topology.

In examining the pros and cons of various topologies discussed, this study introduces a cascaded high gain boost topology that employs two modified boost converters arranged in a cascaded configuration. This innovative design emphasizes key attributes of an effective high gain boost converter, including a high voltage gain, enhanced efficiency, consistent input current, and scalability. The proposed converter delivers a substantial voltage gain at moderate duty cycles, making it well-suited for efficiently elevating low input voltages to higher levels. It achieves notable voltage amplification without requiring extreme duty cycles, which is advantageous for applications with low input voltages. Additionally, the converter ensures the continuity of input current, a crucial factor for

stable operation in low input scenarios such as renewable energy systems, while also minimizing input current ripple. Moreover, the design allows for the cascading of additional cells to further enhance voltage gain, offering adaptability to varying input voltage levels in low input applications. Through the addition of more boosting cells, the converter can be expanded to achieve even greater voltage gains, enhancing its versatility for diverse low input voltage settings.

2. Methodology

2.1 Proposed Configuration and Principle of Operation

Figure 1 illustrates the configuration of the suggested topology, comprising two MOSFETs (M1 and M2), two boosting inductors (L1 and L2), two boosting capacitors (C1 and C2), two boosting diodes (D1 and D2), one rectification diode (D_o), and one output capacitor (C_o). The input voltage (V_{in}) is sourced from a low voltage supply, making it suitable for low energy harvesting devices like fuel cells and solar power modules in this design.

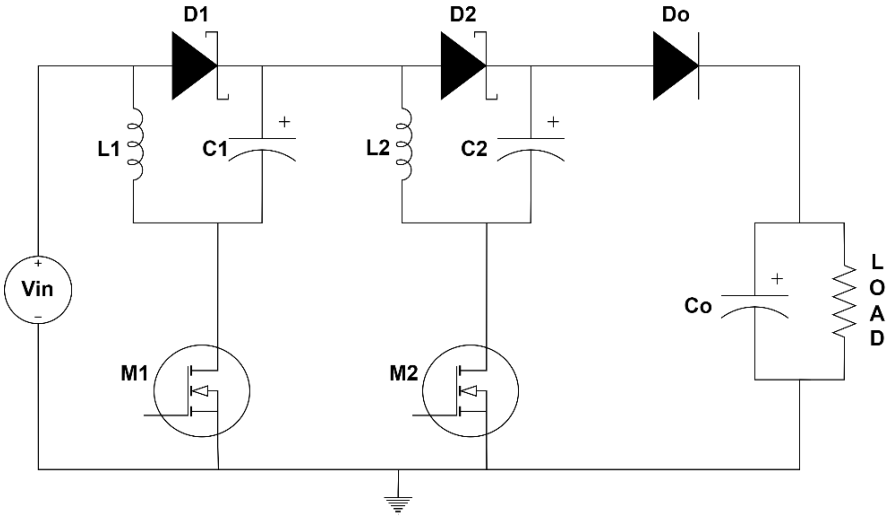

Fig. 1. Schematic circuit of the proposed topology

In this configuration, the two switching MOSFETs (M1 and M2) are tasked with managing the charging and discharging of the boosting cell components (L1-C1 and L2-C2) to elevate the low initial power supply to a higher output level. M1 and M2 operate concurrently with similar gate controls for both activation and deactivation processes. The design presents two distinct modes: Mode 1, which occurs when M1 and M2 are in the ON state, and Mode 2, which is active when both switching MOSFETs are in the OFF state. Figures 2 and 3 illustrate the conduction modes, showcasing the active and inactive components during operation, with inactive components depicted in gray and current paths indicated by red arrows.

Mode 1 ($0 \leq t \leq DT$):

When M1 and M2 are in the ON state as illustrated in Figure 2, the energy from the input voltage V_{in} is stored in the boosting cell components L1-C1 and L2-C2. During this period, the rectifier diode D_o is reverse biased, preventing energy transfer to C_o and the load. However, any initial energy present in C_o at this time will be directed to the load. The red arrows indicate the current flow path in Mode 1, where the load is clearly isolated from the input source. Additionally, the voltage across L1-C1 and L2-C2 is equal to the input supply voltage.

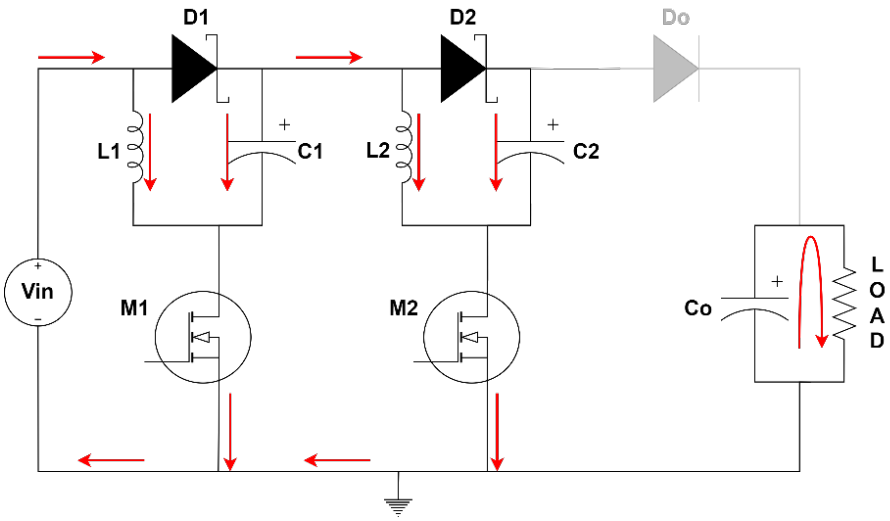

Fig. 2. Circuit operation in MODE 1

Eq. (1) shows the voltage interrelation among all components in Mode 1, with V_{L1}' representing the voltage across the L1 inductor, V_{L2}' denoting the voltage across the L2 inductor, V_{C1}' indicating the voltage across the C1 capacitor, and V_{C2}' representing the voltage across the C2 capacitor, and V_{in} is the input supply voltage.

$$V_{in} = V'_{L_1} = V'_{C_1} = V'_{L_2} = V'_{C_2} \tag{1}$$

The total current in Mode 1 can be expressed in a simplified form as shown in Eq. (2), where I' represents the total current during the ON state. I_{L1}' denotes the current in the L1 inductor, I_{L2}' represents the current in the L2 inductor, I_{C1}' signifies the current in the C1 capacitor, and I_{C2}' indicates the current in the C2 capacitor.

$$I' = I'_{L_1} + I'_{C_1} + I'_{L_2} + I'_{C_2} \tag{2}$$

The ripple current of L1 inductor denoted as ΔI_{L1}' can be determined using Eq. (3) where D is the duty cycle, and T is the switching period.

$$\Delta I'_{L_1} = \frac{V_{in}}{L_1} * DT \tag{3}$$

Similarly for L2, the ripple current denoted as ΔI_{L2}' is represented by Eq. (4).

$$\Delta I'_{L_2} = \frac{V_{in}}{L_2} * DT \tag{4}$$

Mode 2 (DT≤ t ≤ T):

When M1 and M2 are deactivated, as illustrated in Figure 3, the boosting cell components L1-C1 and L2-C2 will be reconfigured into a series connection. The flow of current during this phase is indicated by the red arrows. The rectifier diode D_o is now in a forward bias state, enabling the transfer of stored energy from all boosting elements to the load and facilitating the charging of C_o to its full capacity.

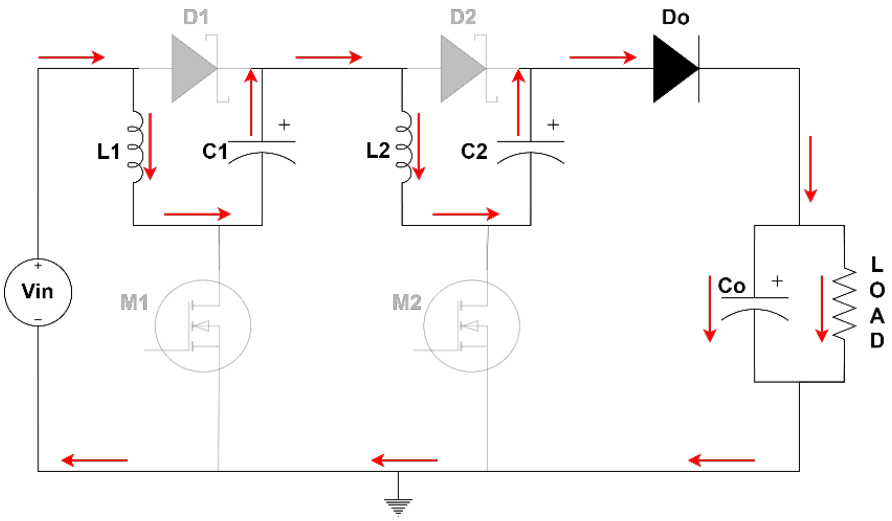

Fig. 3. Circuit operation in MODE 2

Eq. (5) illustrates the voltage interrelation among various components in Mode 2, with V_{Co} representing the output voltage across the C_o capacitor, V_{L1}'' denoting the voltage across the L1 inductor, V_{L2}'' indicating the voltage across the L2 inductor, V_{C1}'' representing the voltage across the C1 capacitor, and V_{C2}'' signifying the voltage across the C2 capacitor and V_{out} is the voltage across the load.

$$V_{in} + V_{L_1}'' + V_{C_1}'' + V_{L_2}'' + V_{C_2}'' = V_{C_o} = V_{out} \tag{5}$$

In Mode 2, the current conduction path is illustrated by Eq. (6), where I'' signifies the total current in the OFF state, I_{Co} represents the current in the C_o capacitor, and I_{out} denotes the load current. Throughout this phase, a similar total current I'' flows through both L1-C1 and L2-C2 cells.

$$I'' = I_{C_o} + I_{out} \tag{6}$$

During this OFF state interval, the ripple current of L1 inductor denoted as $\Delta I_{L1}''$ can be determined using Eq. (7) where D is the duty cycle, and T is the switching period.

$$\Delta I_{L_1}'' = \frac{V_{out} - 4V_{in}}{L_1} * (1 - D)T \tag{7}$$

Similarly for L2, the ripple current denoted as $\Delta I_{L2}''$ is represented by Eq. (8).

$$\Delta I_{L_2}'' = \frac{V_{out} - 4V_{in}}{L_2} * (1 - D)T \tag{8}$$

Applying volt-sec balance principle for L1 inductor resulted in Eq. (9), and for L2 inductor in Eq. (10).

$$\frac{V_{in}}{L_1} * DT = \frac{V_{out} - 4V_{in}}{L_1} * (1 - D)T \tag{9}$$

$$\frac{V_{in}}{L_2} * DT = \frac{V_{out} - 4V_{in}}{L_2} * (1 - D)T \tag{10}$$

Voltage gain, M of the proposed design can be calculated using Eq. (11).

$$M = \frac{V_{out}}{V_{in}} \tag{11}$$

By solving Eq. (9) or Eq. (10), voltage gain along with the duty cycle can be further simplified using Eq. (12).

$$M = \frac{V_{out}}{V_{in}} = \frac{(4-3D)}{(1-D)} \tag{12}$$

2.2 Design Considerations

The appropriate choice of inductors and capacitors is essential for ensuring the continuous conduction mode (CCM) of the proposed circuit. The minimum inductor value can be determined by utilizing Eq. (13), which factors in the allowable inductor ripple percentage (ΔI_L) and the load resistance (R_L). In practical scenarios, the ΔI_L is typically constrained within a range of 30% to 40% to promote safe operational conditions. The values assigned to inductors L1 and L2 are comparable in this design.

$$L_1 = L_2 = \frac{D(3-D)}{(\Delta I_L)M^2} * R_L T \tag{13}$$

To determine the C1 and C2 value, it can be calculated using Eq. (14) where ΔV_C represents the permissible ripple percentage in the capacitor, typically maintained at a level lower than 5% in practical applications.

$$C_1 = C_2 = \frac{M^2 T}{(\Delta V_C)R_L} * \frac{(1-D)}{(3-D)} \tag{14}$$

The minimum output capacitance C_o can be calculated using Eq. (15).

$$C_o = \frac{(1-D)T}{(\Delta V_C)R_L} * \left(\frac{M}{(3-D)} - 1\right) \tag{15}$$

2.3 Design Specifications

In this proposed design, a 12 V low input is utilised at a switching frequency of 50 kHz to elevate the output level to 96 V, with an output power rating of 100 W. Using Eq. (11), the voltage gain of the design can be calculated as:

$$M = \frac{V_{out}}{V_{in}} = 8$$

The duty cycle can be calculated by applying Eq. (12), resulting in a value of D = 0.8. Eq. (13) can then be utilised to determine the critical inductance value required for L1 and L2 to achieve an output power of 100 W where ΔI_L is set at 40% maximum ripple. In practical terms, a larger inductance value must be chosen for the hardware to safely function in continuous conduction mode.

$$L_1 = L_2 = \frac{0.8(3-0.8)}{0.4*8^2} * \frac{92.2}{50^3} = 126\mu H$$

Similarly, for C1 and C2, the capacitance value can be calculated using Eq. (14) where ΔV_C is filtered at 2%.

$$C_1 = C_2 = \frac{(8^2)}{(0.02)(92.2)(50^3)} * \frac{(1-0.8)}{(3-0.8)} = 63.2\mu F$$

Using Eq. (15), the minimum output capacitance value for C_o can be calculated and the practical value can be increased further to eliminate the output voltage ripple.

$$C_o = \frac{(1-0.8)}{(0.02)(92.2)(50^3)} * \left(\frac{8}{(3-0.8)} - 1\right) = 5.73\mu F$$

Table 1 simplifies the complete electrical characteristics of the proposed 100 W high gain cascaded boost topology design.

Table 1
Electrical parameters of the proposed design

Parameter	Value	Parameter	Value
Input voltage, V_{in}	12 V	Output voltage, V_{out}	96 V
Output current, I_{out}	1.04 A	Output power, P_{out}	100 W
Switching period, T	20 µs	Duty cycle, D	0.8
Inductance L_1 and L_2	126 µH	Capacitance C_1 and C_2	63.2 µF
Capacitance C_o	5.73 µF	Voltage gain, M	8
ΔI_L	40%	ΔV_C	2%

The electrical properties are utilised for the purpose of emulating the operational characteristics of the design. It is expected that a target high gain value of 10 will be attained at a duty cycle of 0.86, while for an extreme duty cycle of 0.95, the proposed design is capable of achieving a voltage gain of 23. This elevated voltage gain is unattainable through conventional boost converters, particularly when considering a low input power supply in the design. Simulink software is employed to validate the functionality and efficacy of the proposed design by incorporating all the specified electrical parameters detailed in Table 1. The circuit depicted in Figure 4 is employed during the simulation phase to assess the performance and stability of the design.

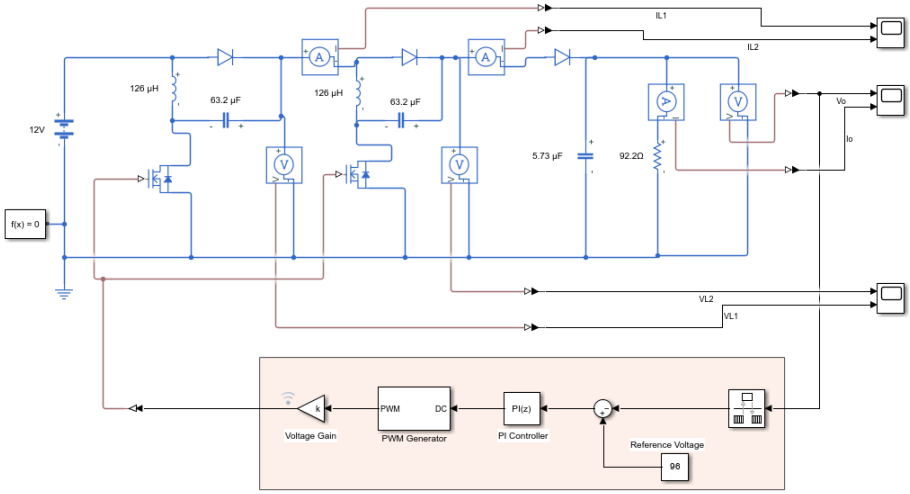

Fig. 4. Simulink schematic for circuit simulation

3. Results and Discussion

The study involves an evaluation of performance and stability utilizing Simulink, with the simulation circuit incorporating electrical parameters outlined in Table 1. Figure 5 presents a comparison of voltage gain and output voltage generation between the proposed converter and three equivalent step up converters (boost, SEPIC, and modified SEPIC) that share a common denominator (1-D) in their voltage gain function. The results depicted in the graph indicate that the proposed topology exhibits notable stability across both low and high duty cycle operations. Notably, starting from a duty cycle of 0.8, the proposed converter demonstrates the ability to achieve a high voltage gain without experiencing abrupt fluctuations in output voltage. This unique characteristic is advantageous in scenarios where consistency and reliability are crucial in the output phase, particularly in contexts requiring precise tuning of duty cycle values. Moreover, the suggested design demonstrates consistent voltage gain stability across a wide range of duty cycles, specifically from 0.2 to 0.7. This suggests resilience in the output stage to potential disturbances, such as abrupt variations in load conditions or switching frequencies, that may arise during operation.

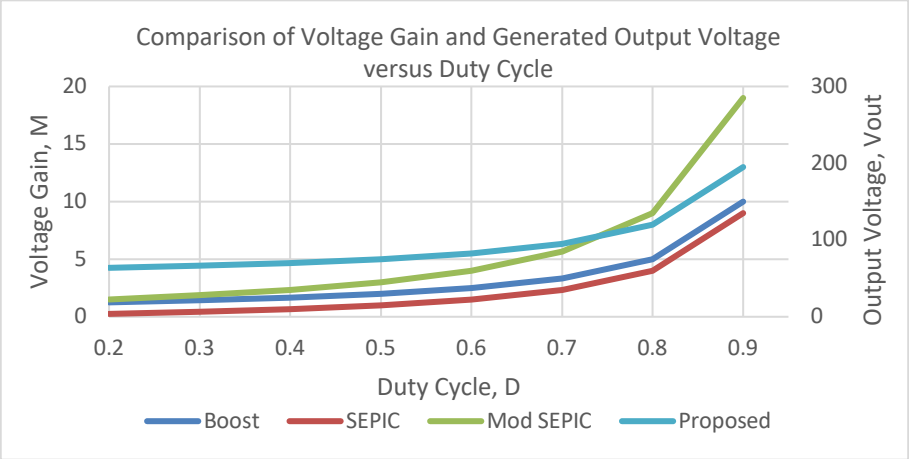

Fig. 5. Comparison of the voltage gain for selected topologies

The simulated waveforms demonstrate effective control over voltage and current, as illustrated in Figure 6. The output voltage stabilizes at the target value of 96 V, while the current reaches a final steady state value of 1.04 A.

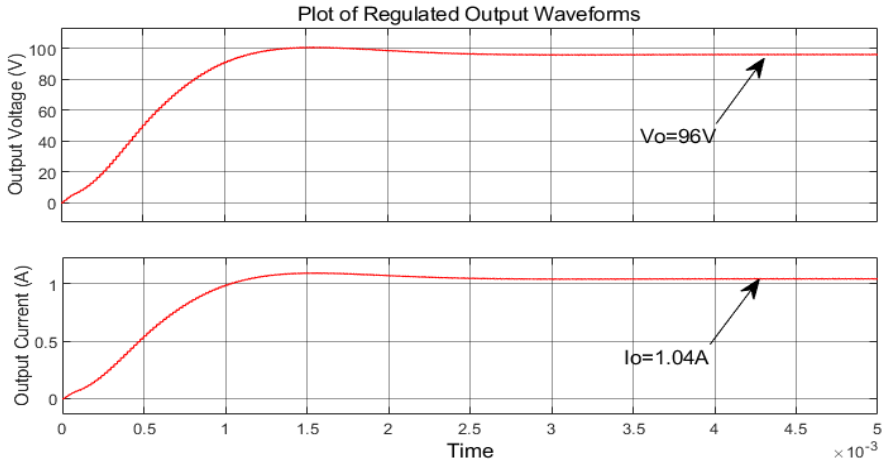

Fig. 6. Plot of the regulated output waveforms

This outcome indicates that the specified critical inductance values for L1 and L2, in conjunction with boosting capacitors C1 and C2, interact effectively with the proposed design to attain the intended output in accordance with the specified duty cycle.

Figure 7 illustrates the peak-to-peak ripple observed in the output voltage and current waveforms. The data indicates a minimal voltage ripple of 0.36 V_{p-p}, representing less than 0.4% deviation, which demonstrates a commendable level of output voltage regulation in comparison to the widely acknowledged standard of less than 5% for output ripple. Similarly, the output current ripple exhibits notable regulation, with a measured ripple of only 5 mA_{p-p} in the output current waveform.

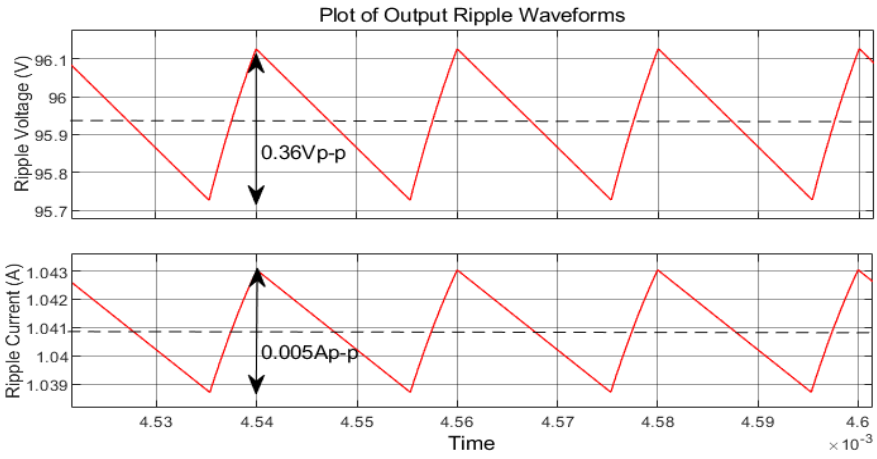

Fig. 7. Plot of the output ripple waveforms

According to the data presented in Table 1, it is necessary to amplify the output voltage to eight times the lower input voltage supply level. To achieve this requirement, the circuit must function in continuous conduction mode (CCM) to create a regulated and highly efficient design. The ability of the proposed design to operate in CCM is clearly illustrated in Figure 8. The current in the L1 inductor consistently conducted in continuous conduction mode. Operating in CCM offers several advantages such as a regulated output, enhanced stability, and reduced output ripple waveforms, as evidenced in Figures 6 and 7 where precise output regulation and minimal output ripple percentage are achieved. The switched voltage across the L1 inductor exhibits a smooth behavior without any spikes or ringing at the desired output level.

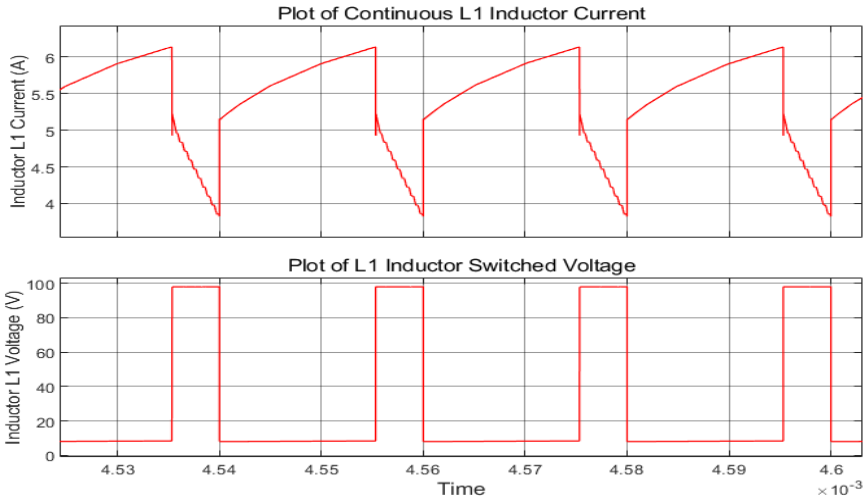

Fig. 8. Plot of L1 inductor current and voltage

4. Conclusions

In this study, a modified boost converter arranged in a cascaded configuration has been successfully developed and evaluated for the purpose of elevating a low input voltage to a higher output level. In contrast to the conventional boost converter topology, this adapted design has demonstrated a notable enhancement in voltage gain when utilised with a comparable duty cycle. Additionally, it exhibits a high level of consistency in response to variations in duty cycle, thereby enhancing its robustness. The control circuit is maintained with a simple single gate drive mechanism to operate the switching MOSFETs. Validation of the proposed design has confirmed its capability to generate a regulated output of 96 V, 1.04 A. The input inductor current, operating in continuous conduction mode, results in minimal output ripple waveforms of less than 0.4% for both output voltage and current.

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